4-CLOCK

100 MHz 64-Bit and 72-bit UNBUFFERED SDRAM DIMM

REVISION 0.8

Changes:

Revision 0.1 April 15, 1997

Preliminary release of 100 MHz spec - Adapted from
"66Mhz 64-bit Unbuffered SDRAM DIMM Specification revision 1.0" combined with "66Mhz 72-bit Unbuffered SDRAM DIMM Specification revision 1.0". Please reference these documents for additional revision information.

Also, inserted information from Intel Preliminary 100Mhz DIMM Layout and Routing Guidelines rev 0.6. Additional content includes SDRAM suggested placement, routing topology diagrams, and trace length tables.

Revision 0.5 April 18, 1997

Post DIMM spec review. Incorporated changes requested at DIMM spec review including: configuration table headings, nominal DIMM height, place holders for mixed mode wiring diagrams, and updated lengths for x16 clocks.

Revision 0.7 June 26, 1997

Follow-up release of 100 Mhz spec - Primary changes include:
Added note to use the latest revision of each "Related Document".
Added corrections to wiring diagrams to include WP pin on EEPROM.
Fixed Wiring diagrams clock loading to match Clock loading table.
Added Wiring diagrams for x16 with ECC and mixed mode DIMMs.
Removed unintentional reference to SOJ on DIMMs, only TSOP are allowed.
Eliminated use of x8 device with x16 devices in the same row.
Added statements addressing 4-layer designs and outer layer clock routing.
Nominal DIMM height removed - only min/max are listed.
Remove extraneous lengths L2 & L3 from clock length table for x16 case.
Added note on under investigation status of x32.
Changed Vcc labeling to Vdd for correctness (except for EEPROM)

Revision 0.8 July 14, 1997

Follow-up release of 100 Mhz spec - Primary changes include:
External Release
Added explanation on DIMM keying
Fixed Mechanical Notes section to include some previously cut-off text.
Added safety section for flammability identification.
Updated EEPROM min storage temperature.
Changed DIMM "bank" references to "row" where appropriate.
Added clarification to DQ/CB min/max total length requirement.
Removed +/10% length requirement on CS & CKE.

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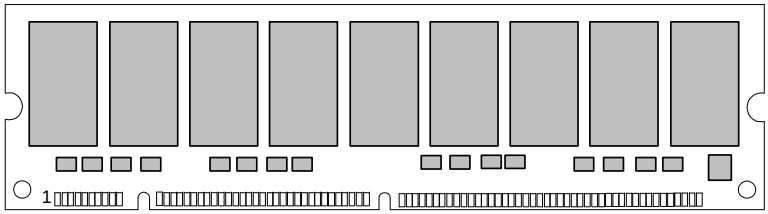
1.0 Introduction

This specification defines the electrical and mechanical requirements for 168-pin, 3.3 volt, 100 MHz, 64-bit and 72-bit wide, 4 clock, unbuffered Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory installed on personal computer motherboards.



This specification largely follows the JEDEC defined 168-pin unbuffered SDRAM DIMM as of JEDEC committee meeting of December 1996.

Related Documents

Table 1: Related Documents

TITLE	REV	DATE
Intel PC/100 SDRAM Specification	1.4	February 1997
Intel SDRAM SPD Data Structure Specification	1.1	April 1997

The related documents contain information that is critical to this specification. The revisions listed are the latest releases at the time of this writing. However, it is important to use the most current revisions of each of these documents when generating or modifying DIMM designs.

DIMM Configurations

SDRAM DIMM configurations are defined in the following tables:

Table 2: SDRAM Non Mixed-Mode Module Configurations

Config #	DIMM Capacity	DIMM Organization	SDRAM density	SDRAM Organization	# of SDRAMs	# Rows of SDRAM	# Banks in SDRAM	# Address bits row/bank/col
1	8 MB	1M X 64	16 Mbit	1MX16	4	1	2	11/1/8
2	16 MB	2M X 64	16 Mbit	1MX16	8	2	2	11/1/8
3	16 MB	2M X 64	16 Mbit	2MX8	8	1	2	11/1/9
4	32 MB	4M X 64	16 Mbit	2MX8	16	2	2	11/1/9
5	16 MB	2M X 64	64 Mbit	2MX32	2	1	4	11/2/8
							2	11/1/9
							2	12/1/8
6	32 MB	4M X 64	64 Mbit	2MX32	4	2	4	11/2/8
							2	11/1/9
							2	12/1/8
7	32 MB	4M X 64	64 Mbit	4MX16	4	1	4	12/2/8
							2	11/1/10
							2	13/1/8
8	64 MB	8M X 64	64 Mbit	4MX16	8	2	4	12/2/8
							2	11/1/10
							2	13/1/8
9	64 MB	8M X 64	64 Mbit	8MX8	8	1	4	12/2/9
							2	13/1/9
10	128 MB	16M X 64	64 Mbit	8MX8	16	2	4	12/2/9
							2	13/1/9
11	16 MB	2M X 72	16 Mbit	2MX8	9	1	2	11/1/9
12	32 MB	4M X 72	16 Mbit	2MX8	18	2	2	11/1/9
13	64 MB	8M X 72	64 Mbit	8MX8	9	1	4	12/2/9
							2	13/1/9
14	128 MB	16M X 72	64 Mbit	8MX8	18	2	4	12/2/9
							2	13/1/9
15	8 MB	1M X 72	16 Mbit	1MX16	5	1	2	11/1/8
16	16 MB	2M X 72	16 Mbit	1MX16	10	2	2	11/1/8
17	32 MB	4M X 72	64 Mbit	4MX16	5	1	4	12/2/8
							2	11/1/10
							2	13/1/8
18	64 MB	8M X 72	64 Mbit	4MX16	10	2	4	12/2/8
							2	11/1/10
							2	13/1/8

Note 1: Modules constructed using x 4 bit SDRAMs are not supported (due to loading on select signals).
Note 2: Modules constructed using x 32 bit SDRAMs are still under investigation. Additional information will be released when it becomes available.

Table 3: SDRAM Mixed-Mode Module Configurations

Config #	DIMM Capacity	DIMM Organization	SDRAM density	SDRAM Organization	# of SDRAMs	# of Rows of SDRAM	Banks in SDRAM	# Address bits row/bank/col
1	24 MB	2M X 64 +	16 Mbit	2MX8	8	2	2	11/1/9
		1M X 64	16 Mbit	1MX16	4		2	11/1/8
2	48 MB	4M X 64 +	64 Mbit	4MX16	4	2	4	12/2/8
							2	11/1/10
							2	13/1/8
		2M X 64	16 Mbit	2MX8	8		2	11/1/9
3	24 MB	2M X 72 +	16 Mbit	2MX8	9	2	2	11/1/9
		1M X72	16 Mbit	1MX16	5		2	11/1/8
4	48 MB	4M X 72 +	64 Mbit	4MX16	5	2	4	12/2/8
							2	11/1/10
							2	13/1/8
		2M X72	16 Mbit	2MX8	9		2	11/1/9
5	96 MB	8M X 72 +	64 Mbit	8MX8	9	2	4	12/2/9
							2	13/1/9
		4M X 72	64 Mbit	4MX16	5		4	12/2/8
								11/1/10
								13/1/8

Note: Modules constructed using x 4 bit SDRAMs are not supported (due to loading on select signals).

Design Stuffing Options

For the purpose of minimizing the total number of card designs that need to be generated, all Intel reference designs are being done double-sided in 6 layers and using this design guide with the intent that these PCB designs will also work for single sided population and with or without stuffing the ECC devices. Therefore, there will be one card each designed for non-mixed mode configuration sets (1,2,15,16) (7,8,17,18) (3,4,11,12) (9,10,13,14). DIMM designs generated outside of Intel using the DIMM design guide may opt not to do the same if cost or other considerations make it undesirable.

Distinction between "banks"

This document refers to two types of "banks". One type relates to the banks of memory internal to the SDRAM component (two or four). The other type relates to the banks of SDRAM on a DIMM, also referred to as "rows". The number of rows is the number of sets of SDRAMs on the DIMM that collectively make up 64 or 72 bits wide of data. When reading this document, please be aware of this distinction.

2.0 Environmental Requirements

The SDRAM DIMM shall be designed to operate within a personal computer cabinet in an office environment with limited capacity for heating and air conditioning. The temperature and humidity limits are listed below.

Table 4: DIMM Temperature, Humidity & Barometric Pressure Requirements

Operating Temperature	0 ^{o}C to +65 ^{o}C ambient
Operating Humidity	10% to 90% relative humidity
Storage Temperature	-50 ^{o}C to + 100 ^{o}C
Storage Humidity	5% to 95% without condensation
Barometric Pressure (operating & storage)	105K - 69K Pascal (up to 9,850 ft.)

Safety - UL Rating

Printed wiring board to have a flammability rating of 94V-O Markings to include UL tractability requirements per *UL Recognized Component Directory.*

3.0 Mechanical Design

The following table and mechanical drawings give the specific dimensions and tolerances for a 168-pin DIMM.

Table 5: DIMM Dimensions and Tolerances

SYMBOL	DEFINITION	MIN	NOM	MAX	NOTES
A	Overall module height measured from Datum -B-.	25.35 mm		38.25 mm	Range is 25.40 mm (1.0") to 38.10 mm. (1.5")
A1	The distance from Datum -B- to the centerline of the PWB alignment holes.	3.00 mm BASIC			These holes are not used by the next level of assembly. The dimensions are supplied for information only. If the holes are used in manufacturing they should be tightly toleranced. The recommended positional tolerance is 0.10 mm.
A2	The distance from Datum -B- to the centerline of the latch holes.	17.80 mm BASIC			
A3	The distance from Datum -B- to the lower edge of the Component Area.	20.80 mm			This distance applies to the Component Area in the latch hole area.
A4	The distance from Datum -B- to the lower edge of the Component Area on the front side of the PWB.	4.00 mm			
A5	The distance from Datum -B- to the lower edge of the Component Area on the back side of the PWB.	4.00 mm			
A6	The distance from Datum -B- to the leading edge of the contact.	0.05 mm		0.35 mm	The minimum distance prevents contact edge burrs.
b	The width of the plated input/output contact measured at the lateral midpoint of the contact.	0.95 mm	1.00 mm	1.05 mm	
D1	The overall length of the PWB.	133.22 mm	133.37 mm	133.52 mm	
D2	The longitudinal distance between the PWB machining alignment hole centers.	126.20 mm	127.35	128.50 mm	These holes are optional and may or may not be present. If they are present, they must be located as defined.

Table 6: DIMM Dimensions and Tolerances (continued)

SYMBOL	DEFINITION	MIN	NOM	MAX	NOTES
e	The pitch or distance between centerlines of the contacts		1.27 mm BASIC		
e1	The distance between the centerlines of Contact 1 and 84.		115.57 mm		
e2	The distance between the centerlines of Contact 85 and 168.		115.57 mm		
e3	The distance between the centerlines of Contact 1 and the contact located at the immediate left of the left key zone when viewing contact 1 side.		11.43 mm		The distance between the centerlines of contact 1 and 10.
e4	The distance between the centerlines of the contact at the immediate right of the left key zone and the contact at the immediate left of the center key zone when viewing contact 1 side.		36.83 mm		The distance between the centerlines of contact 11 and 40.
e5	The distance between the centerlines of the contact located at the immediate right of the center key zone and contact 84.		54.61 mm		The distance between the centerlines of contact 41 and 84.
H	The diameter of the PWB machined alignment holes.	2.90 mm	3.00 mm	3.10 mm	The machined alignment holes are optional.
L	The distance from Datum -B- to the top edge of the plated contact.	2.30 mm	2.50 mm	2.70 mm	
N	The total number of contacts.		168		
T	The thickness of the PCB including the contact metalization and plating.	1.17 mm	1.27 mm	1.37 mm	
T1	The overall thickness of the PWB with the components mounted. The overall thickness is measured from the highest component on the front side to the highest component on the backside.			4.00 mm	
aaa	The positional tolerance for the overall body length D1.	aaa = 0.15 mm @ Maximum Material Condition			
bbb	The straightness tolerance for the card thickness including the metalized contacts. This callout applies to the zone defined by A4, A5 and D1.		0.40 mm		bbb = 0.3% x D1 rounded to a two decimal place hard metric value.
ccc	The positional tolerance for the pattern of contacts with regard to primary Datum -A-.	ccc = 0.10 mm @ Least Material Condition			
ddd	The positional tolerance for the individual contact width b with regard to the theoretical centerline of the contact defined by basic dimension e.	ddd = 0.05 mm @ Least Material Condition			

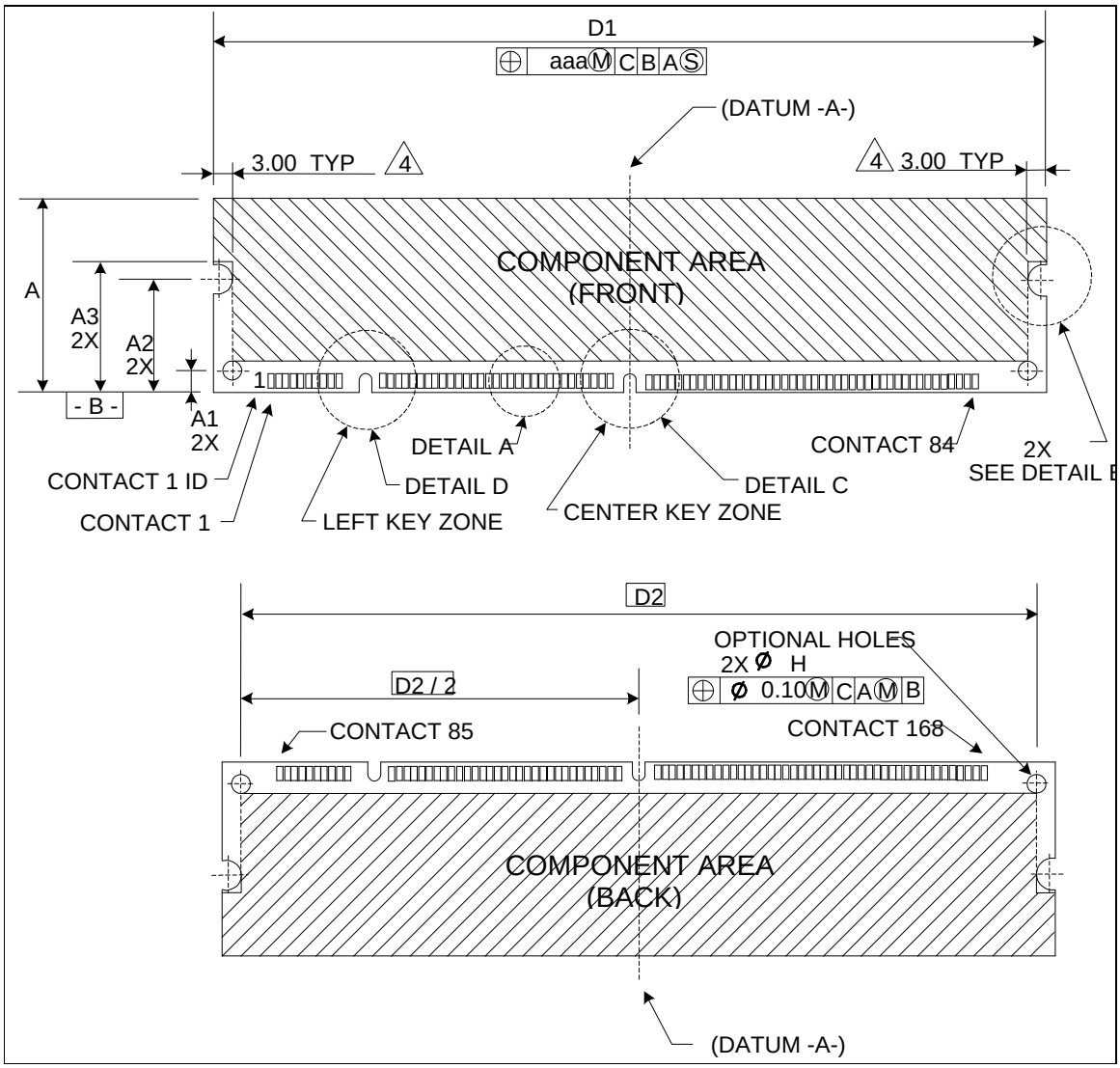


Figure 1: DIMM Mechanical Drawing (1 of 5)

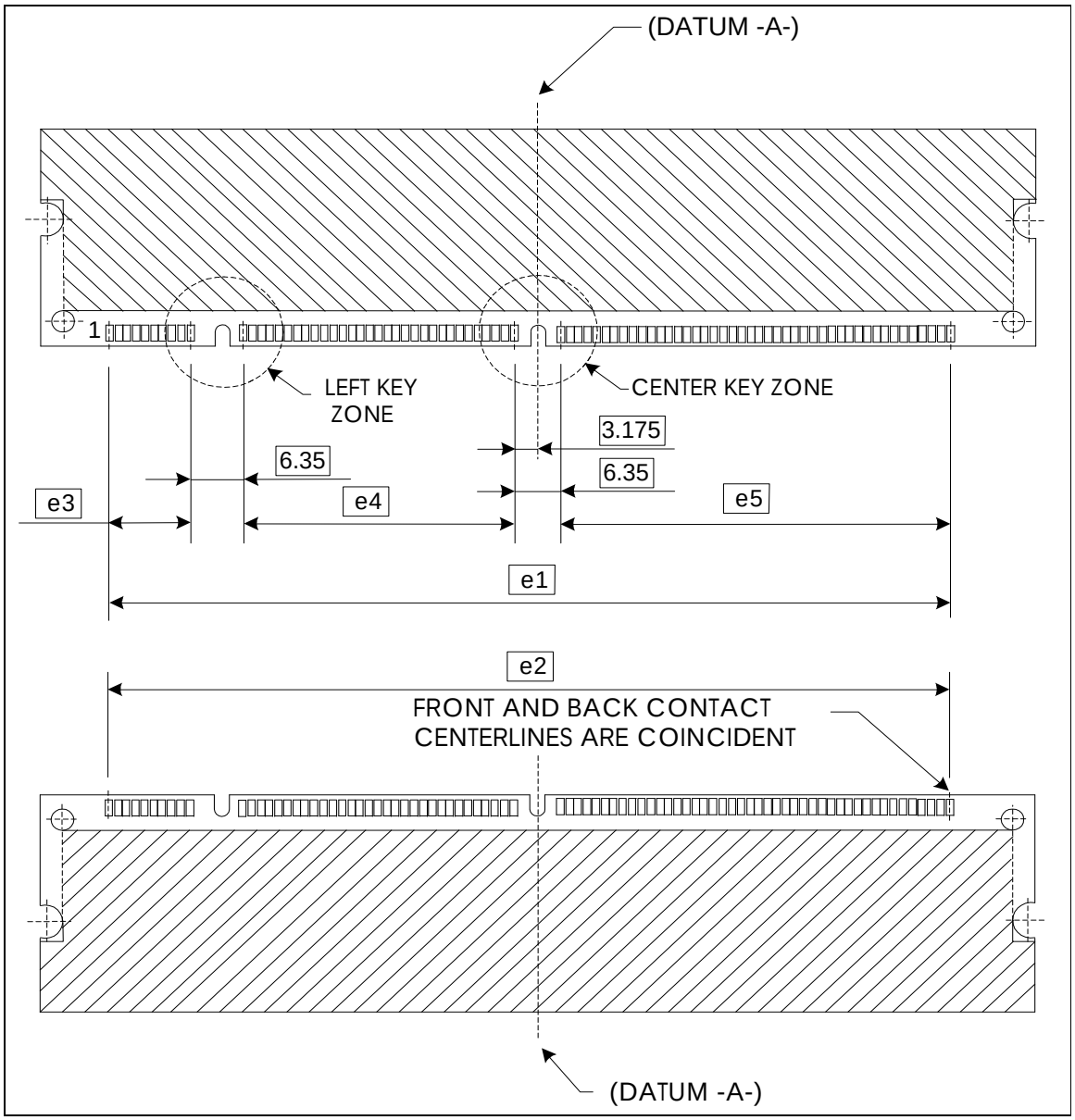


Figure 2: DIMM Mechanical Drawing (2 of 5)

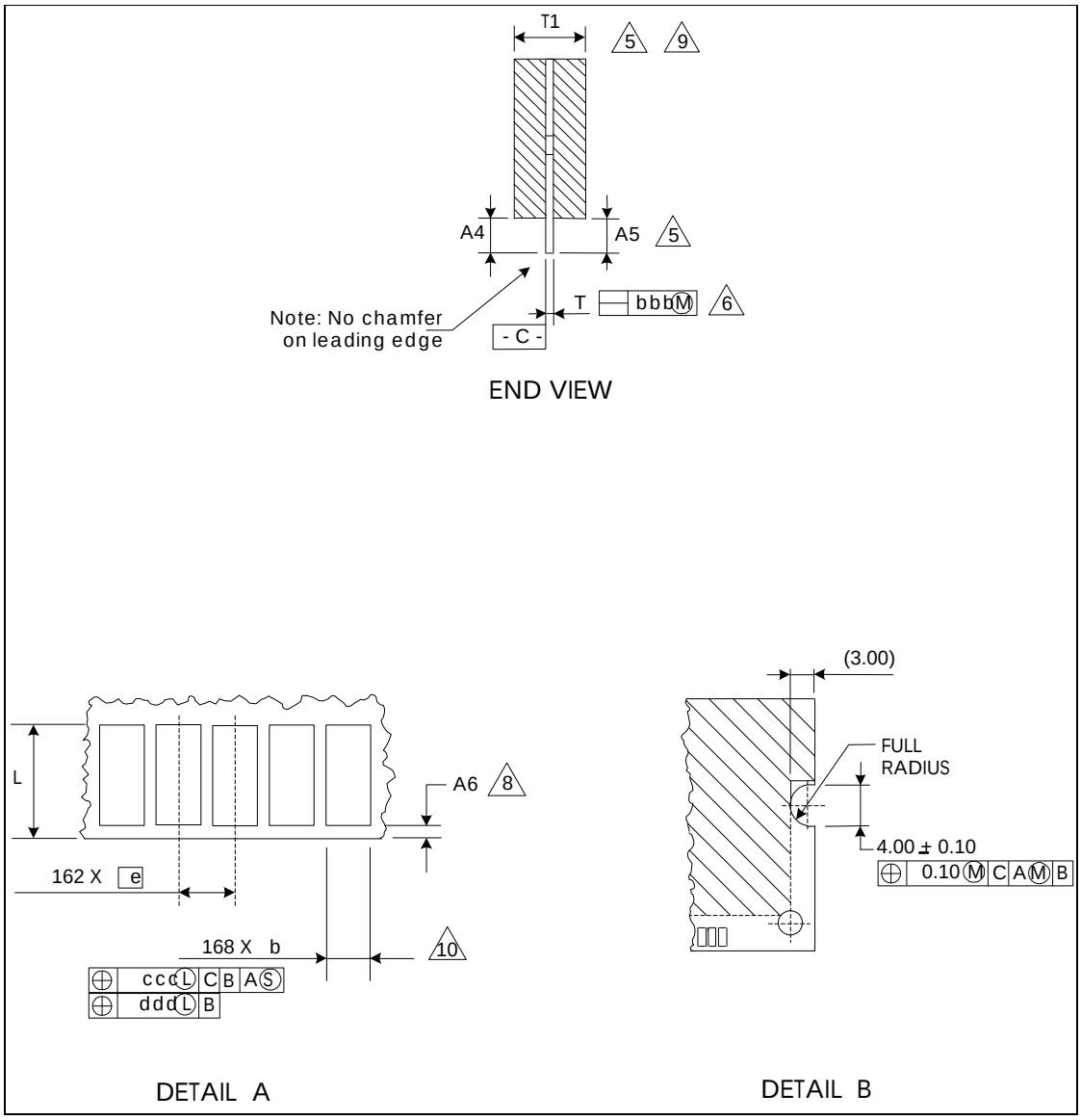


Figure 3: DIMM Mechanical Drawing (3 of 5)

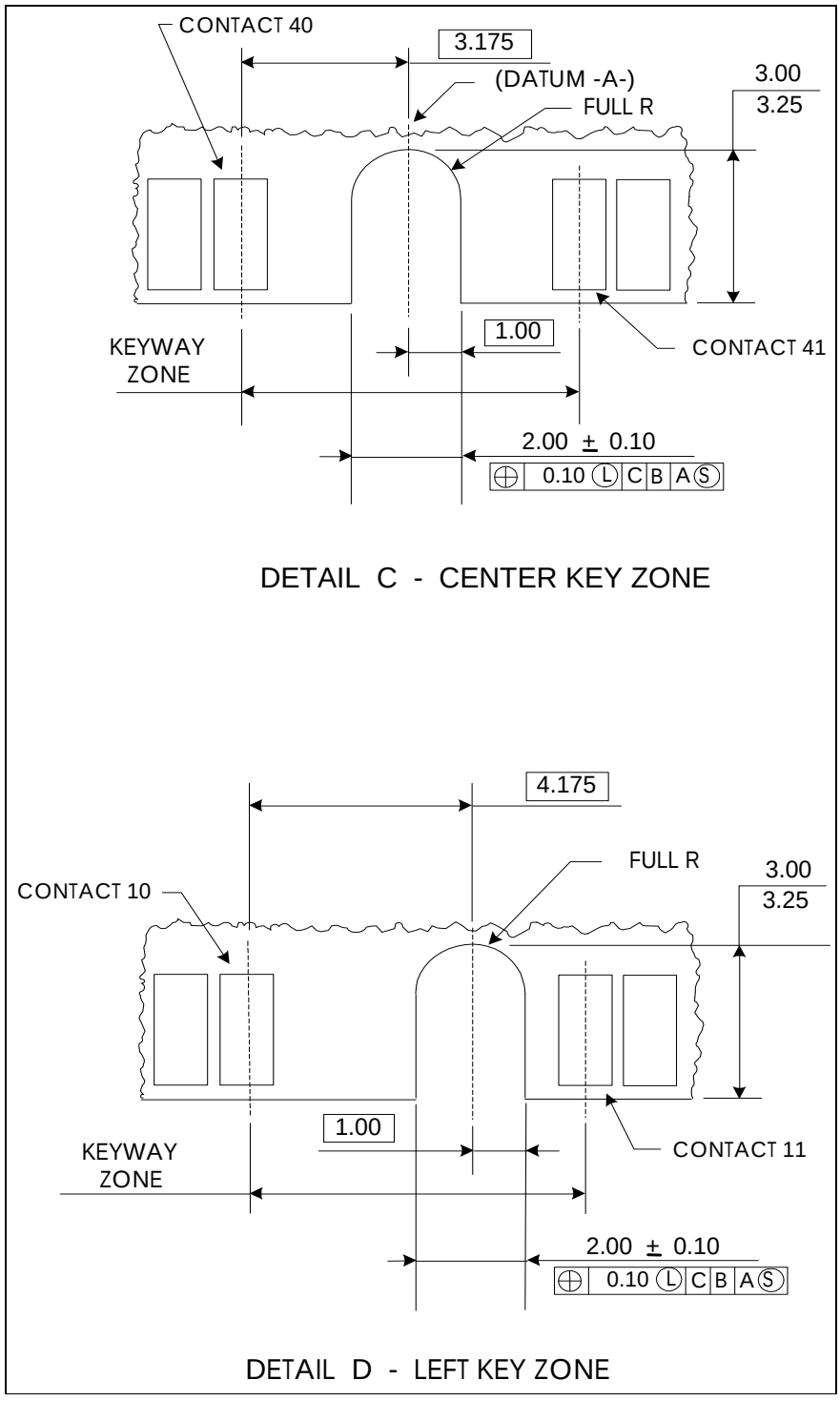


Figure 4: DIMM Mechanical Drawing (4 of 5)

NOTES

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994.

2 TOLERANCES ON ALL DIMENSIONS +/- 0.13 UNLESS OTHERWISE SPECIFIED.

3 ALL DIMENSIONS ARE IN MILLIMETERS.

4 3.00 mm TYPICAL APPLIES TO BOTH 4.00 mm WIDE NOTCH LENGTH AND COMPONENT KEEPOUT AREA.

5 DIMENSION APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH SIDES.

6 CARD THICKNESS APPLIES ACROSS THE CONTACTS AND INCLUDES PLATING AND/OR METALIZATION. STRAIGHTNESS CALLOUT APPLIES TO ZONE DEFINED BY A4, A5, AND D1.

7 N IS THE TOTAL NUMBER OF CIRCUIT CONTACTS (PINS, LEADS, TABS OR PADS).

8 LEADING EDGE OF CONTACT ZONE SHALL BE FREE OF BURRS AND EXTERNAL TIE BARS.

9 THE MAXIMUM THICKNESS SHALL NOT EXCEED 4.00 mm.

APPLICATION NOTES:

10 PLATING FOR CONTACT PADS: GOLD PLATING 0.75 MICROMETER MINIMUM OVER NI PLATING 2 MICROMETERS MINIMUM.

11 FOR OPTIMUM PERFORMANCE, IT IS RECOMMENDED THAT THE TIEBAR BE OFFSET FROM THE CENTERLINE OF THE PAD. ALSO, THE TIEBAR MAY BE AN INTERNAL LAYER, SO THE REMNANT CANNOT CAUSE CONTACT DAMAGE.

Figure 5: DIMM Mechanical Drawing (5 of 5)

Explanation of DIMM Keying

All DIMMs generated from this spec should have two notches cut into the edge connection that convey information on the voltage of the DIMM and whether it is buffered or unbuffered. One notch should be positioned between DIMM pins 10 and 11 and should be closer in proximity to pin 11. This signifies that the DIMM is Unbuffered SDRAM/DRAM. The other notch should be positioned between DIMM pins 40 and 41 and should be centered between the two pins. This signifies that the DIMM operates using a Vddq voltage of 3.3 Volts. Please see the mechanical drawings above for exact dimensions and placement of these notches.

4.0 Module Pinout

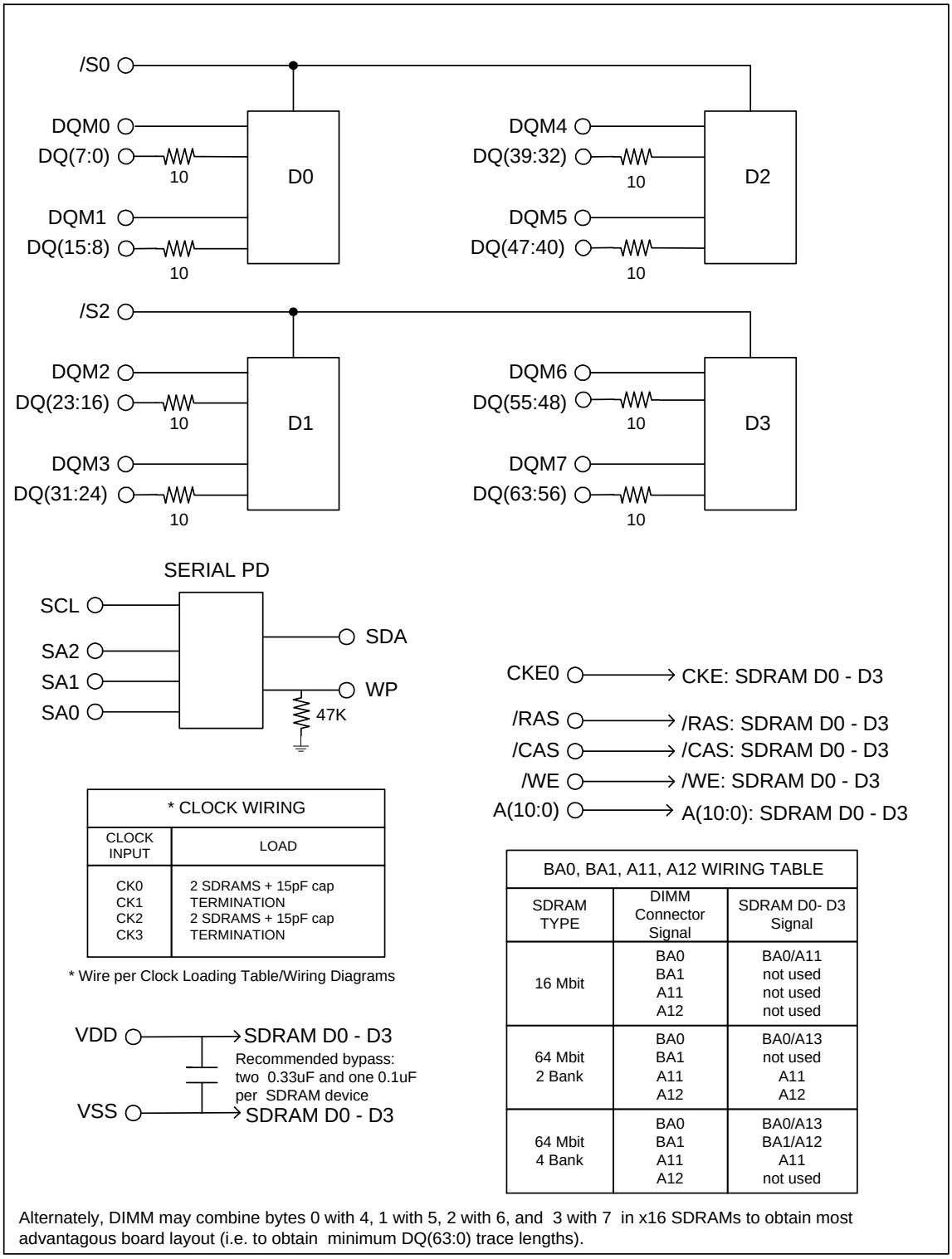
The following table provides the 168-pin 64-bit and 72-bit unbuffered DIMM module connector pinouts. Note that the eight error detection and correction bits CB(0:7) are actually NC for the 64-bit pinout.

Table 7: SDRAM DIMM pinout

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	/S3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vdd	48	NC	90	Vdd	132	A13
7	DQ4	49	Vdd	91	DQ36	133	Vdd
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vdd	101	DQ45	143	Vdd
18	Vdd	60	DQ20	102	Vdd	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vdd	68	Vss	110	Vdd	152	Vss
27	/WE0	69	DQ24	111	/CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/S0	72	DQ27	114	/S1	156	DQ59
31	NC	73	Vdd	115	/RAS	157	Vdd
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	Vdd	82	SDA	124	Vdd	166	SA1
41	Vdd	83	SCL	125	CK1	167	SA2
42	CK0	84	Vdd	126	A12	168	Vdd

Note: NC = Not Connected

5.0 SDRAM DIMM Block Diagrams



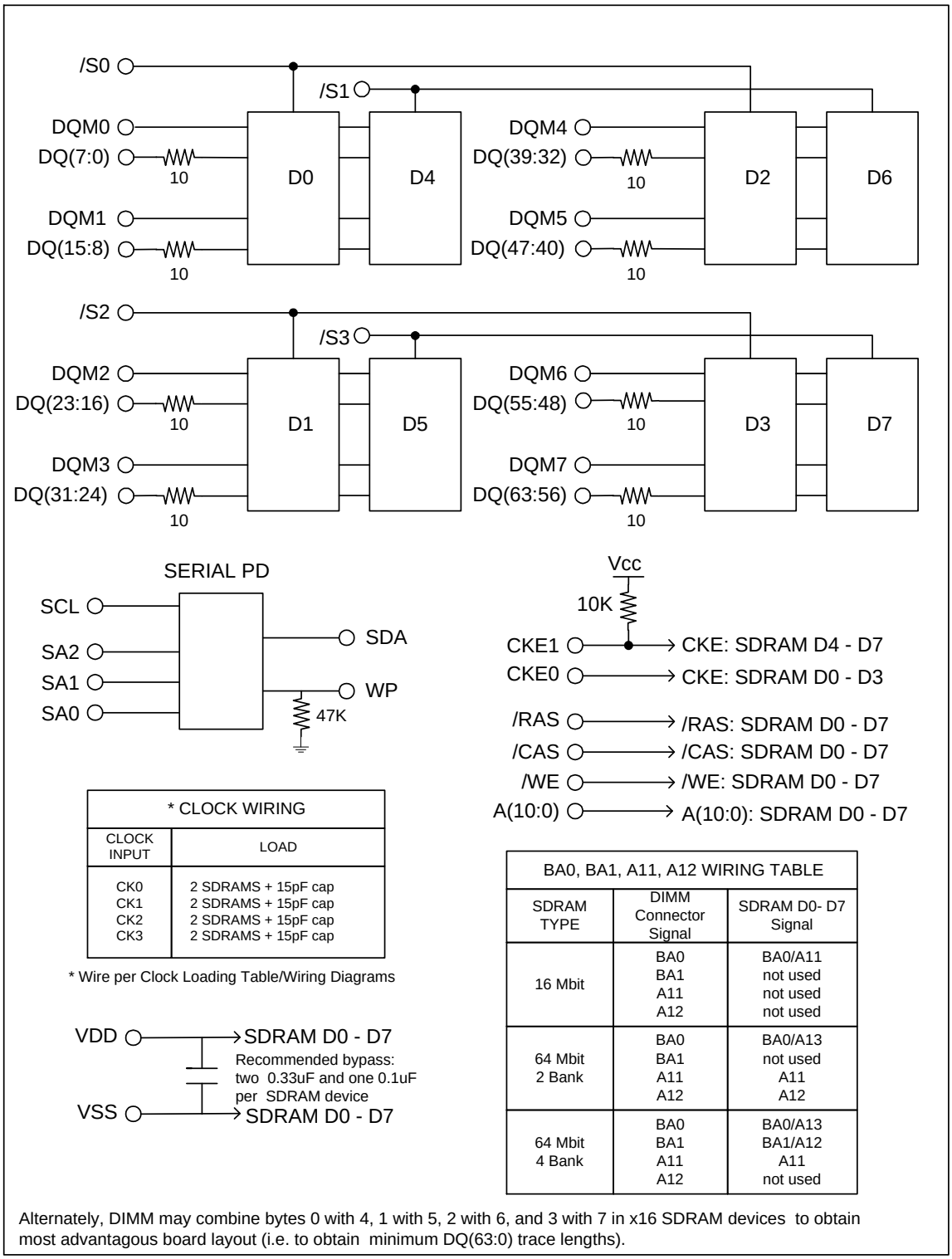
* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	2 SDRAMS + 15pF cap TERMINATION 2 SDRAMS + 15pF cap TERMINATION

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0- D3 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Alternately, DIMM may combine bytes 0 with 4, 1 with 5, 2 with 6, and 3 with 7 in x16 SDRAMs to obtain most advantagous board layout (i.e. to obtain minimum DQ(63:0) trace lengths).

Figure 6: 1 Row, x16 SDRAMs DIMM Block Diagram



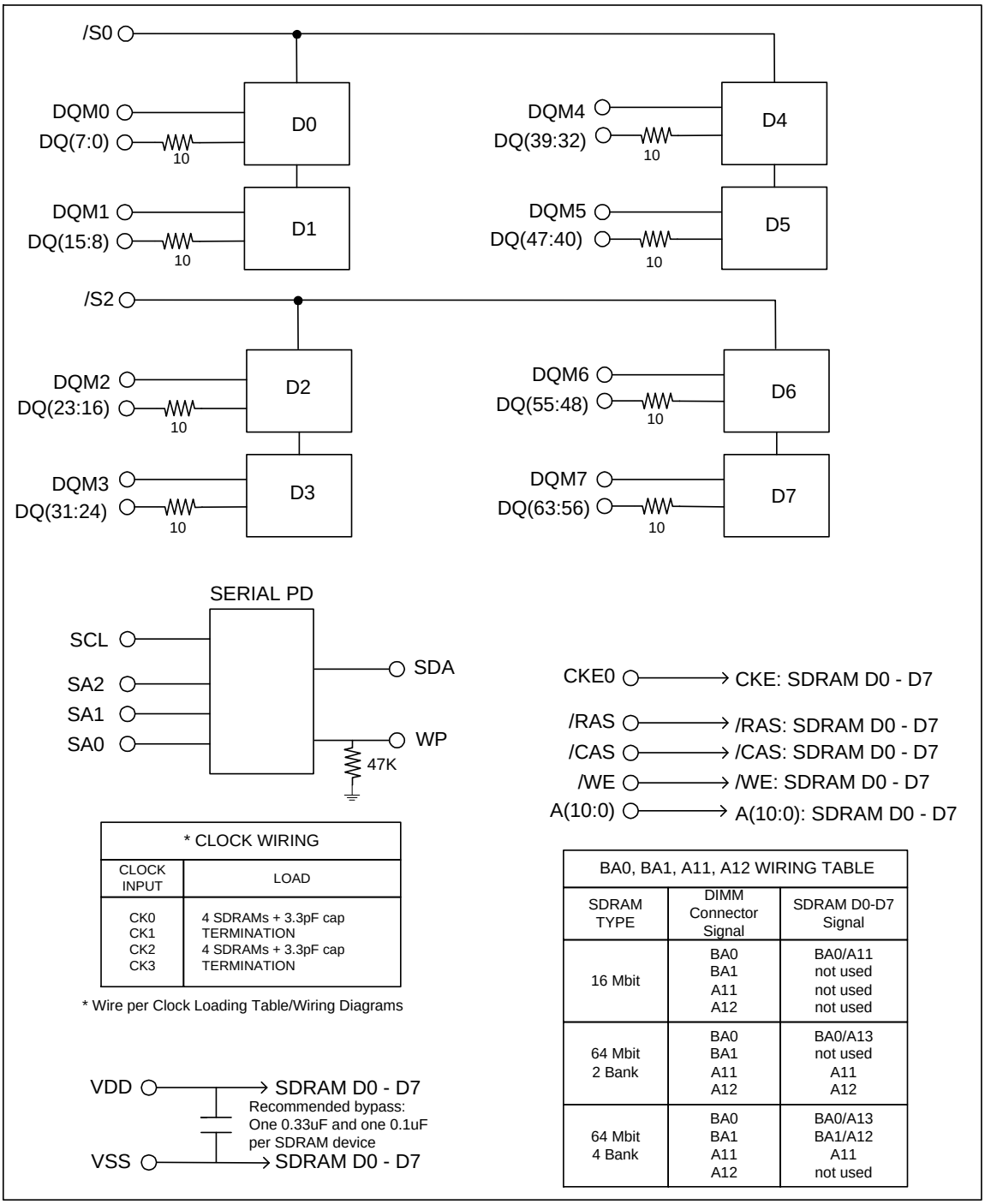
* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	2 SDRAMS + 15pF cap 2 SDRAMS + 15pF cap 2 SDRAMS + 15pF cap 2 SDRAMS + 15pF cap

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0- D7 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Alternately, DIMM may combine bytes 0 with 4, 1 with 5, 2 with 6, and 3 with 7 in x16 SDRAM devices to obtain most advantagous board layout (i.e. to obtain minimum DQ(63:0) trace lengths).

Figure 7: 2 Rows, x16 SDRAMs DIMM Block Diagram

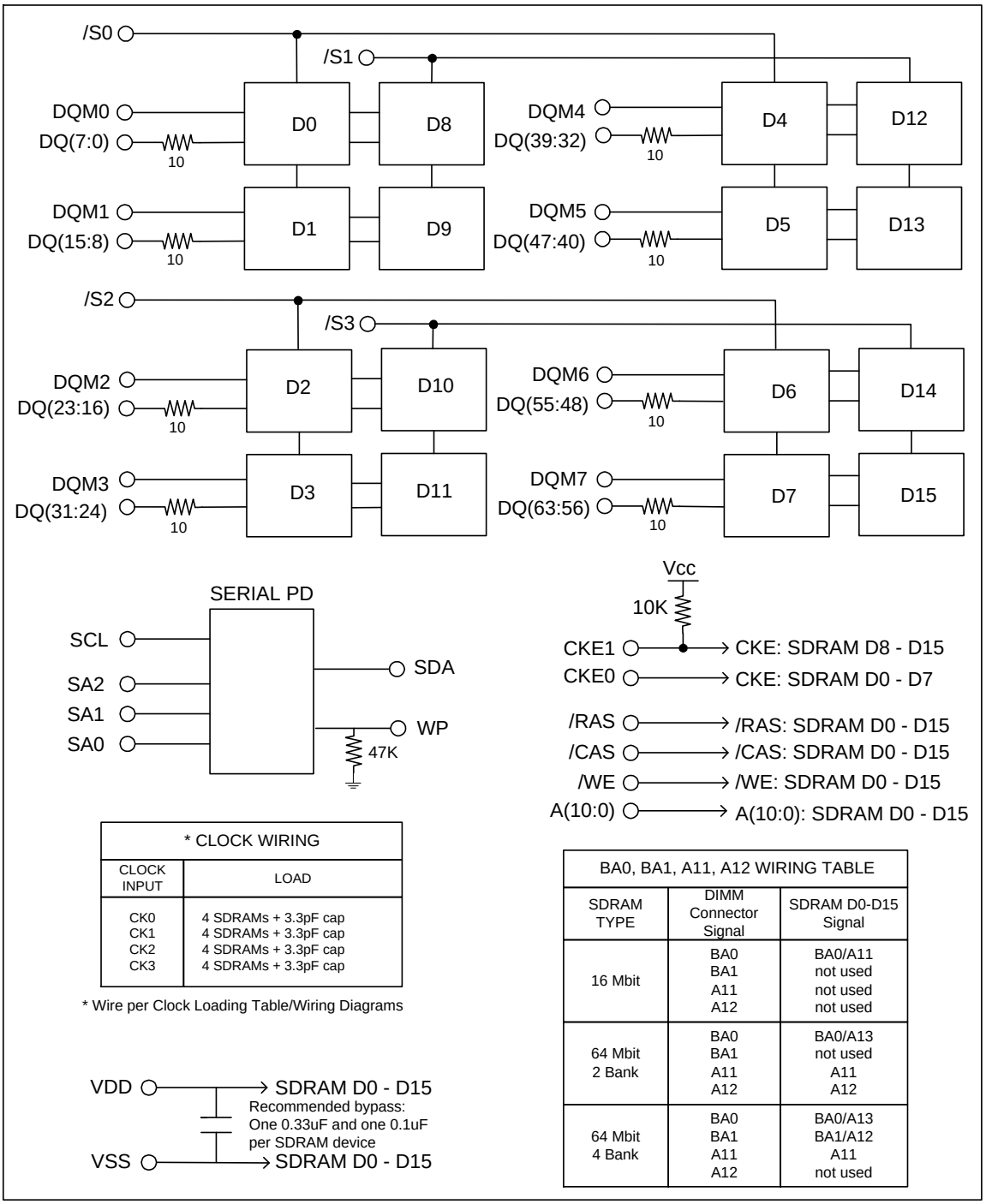


* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	4 SDRAMs + 3.3pF cap TERMINATION 4 SDRAMs + 3.3pF cap TERMINATION

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0-D7 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Figure 8: 1 Row x8 SDRAMs DIMM Block Diagram

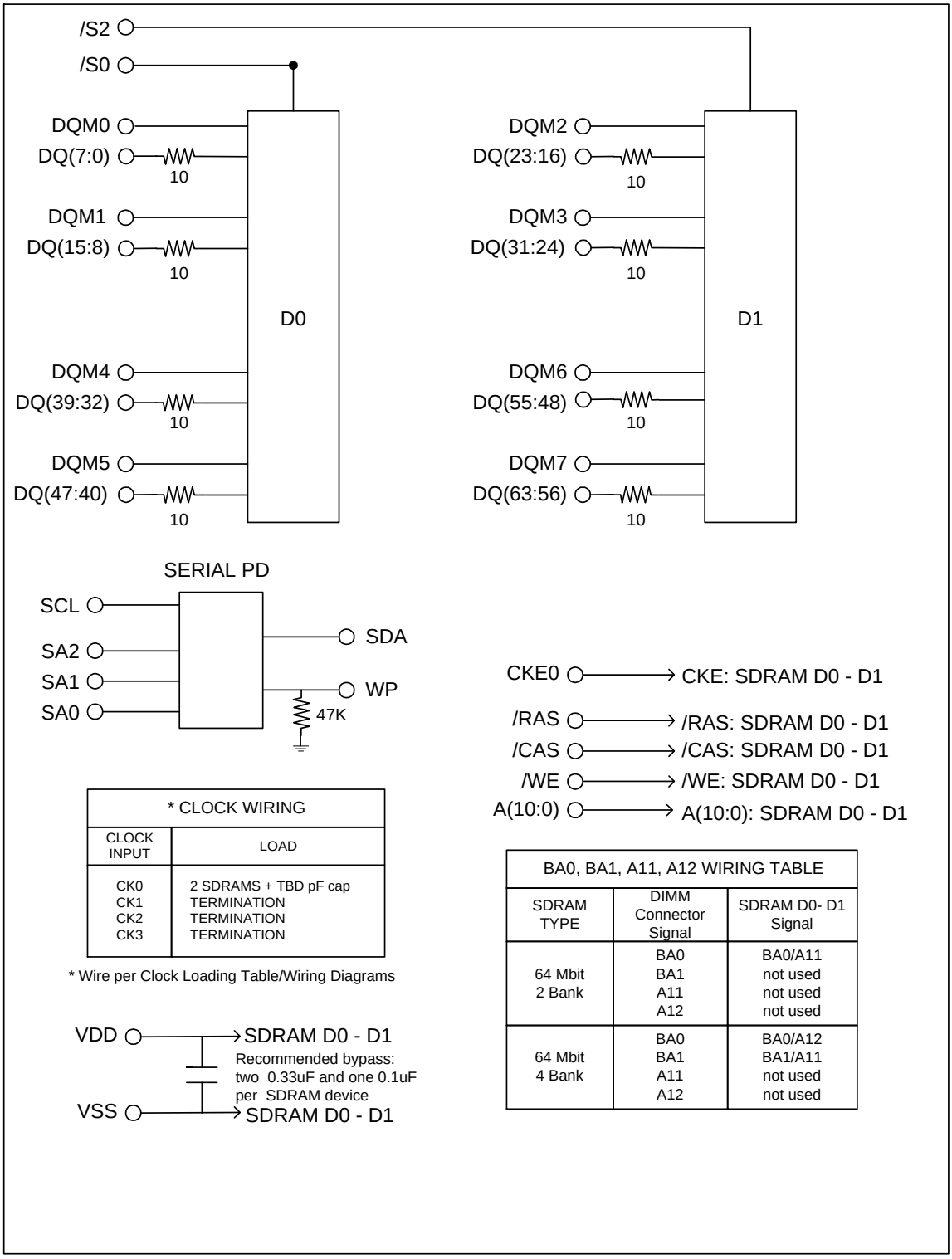


* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	4 SDRAMs + 3.3pF cap 4 SDRAMs + 3.3pF cap 4 SDRAMs + 3.3pF cap 4 SDRAMs + 3.3pF cap

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0-D15 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Figure 9: 2 Rows x8 SDRAMs DIMM Block Diagram

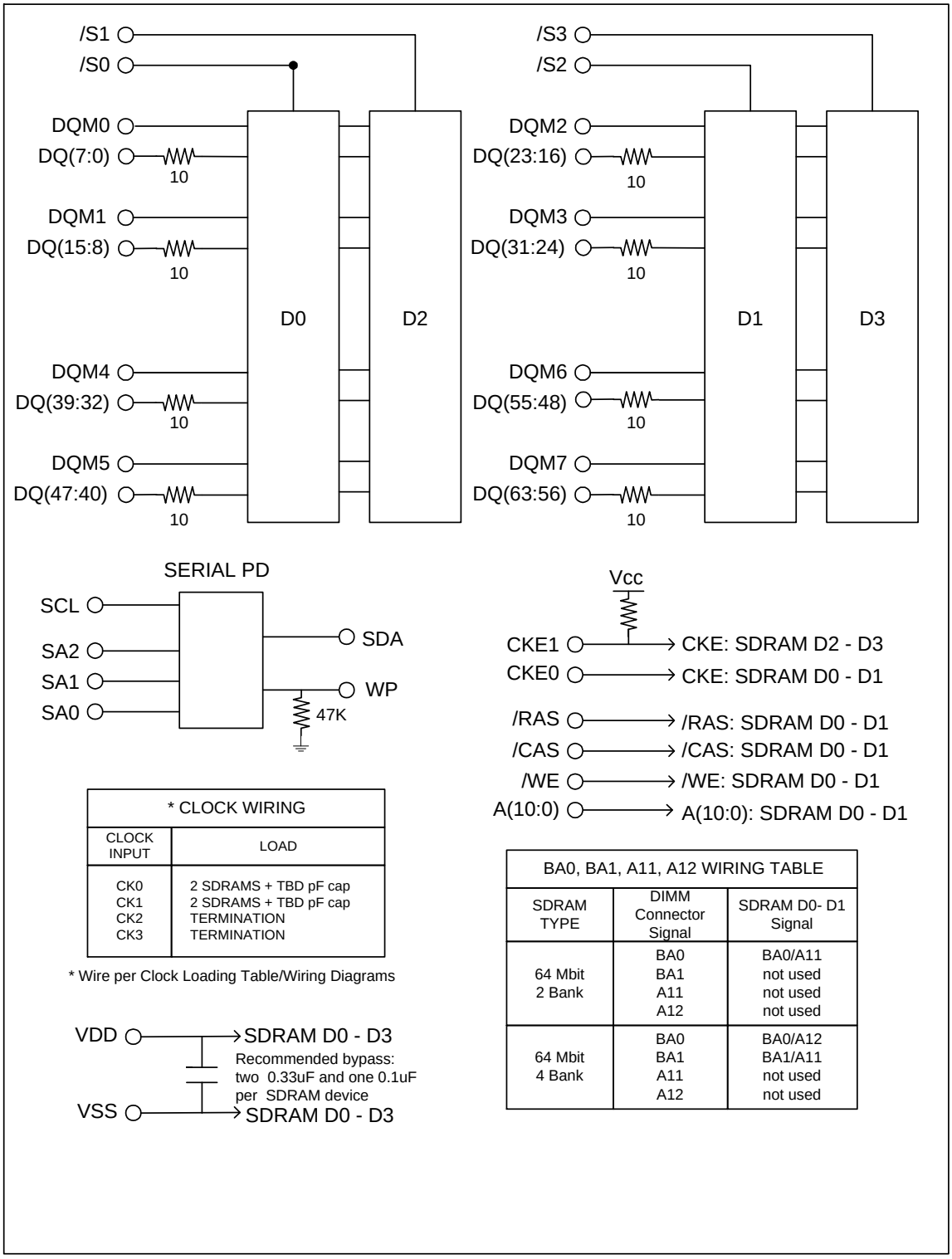


* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	2 SDRAMS + TBD pF cap TERMINATION TERMINATION TERMINATION

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0- D1 Signal
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A12 BA1/A11 not used not used

Figure 10: 1 Row x 32 SDRAMs Block Diagram

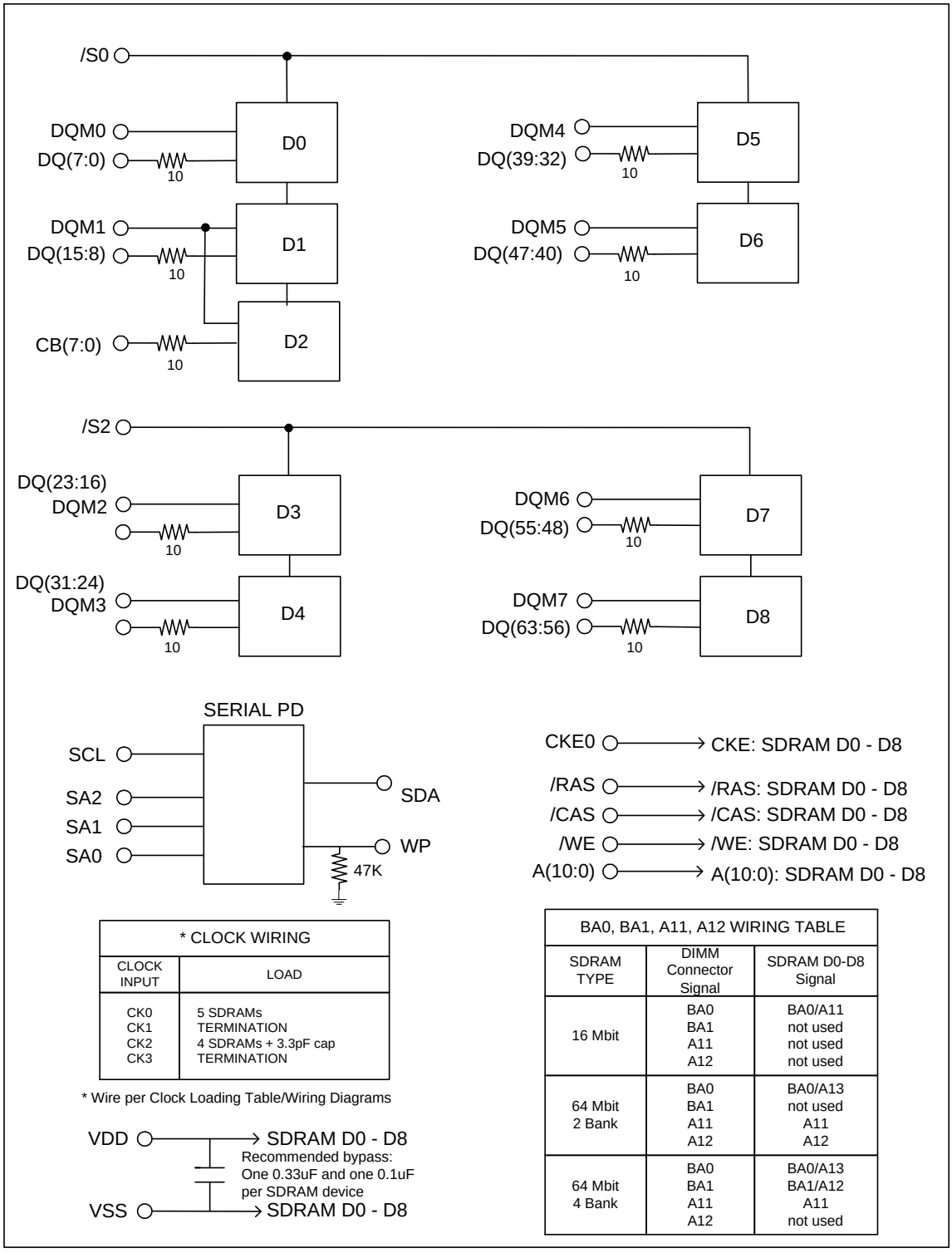


* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0	2 SDRAMS + TBD pF cap
CK1	2 SDRAMS + TBD pF cap
CK2	TERMINATION
CK3	TERMINATION

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0- D1 Signal
64 Mbit 2 Bank	BA0	BA0/A11
	BA1	not used
	A11	not used
	A12	not used
64 Mbit 4 Bank	BA0	BA0/A12
	BA1	BA1/A11
	A11	not used
	A12	not used

Figure 11: 2 Rows x32 SDRAMs Block Diagram

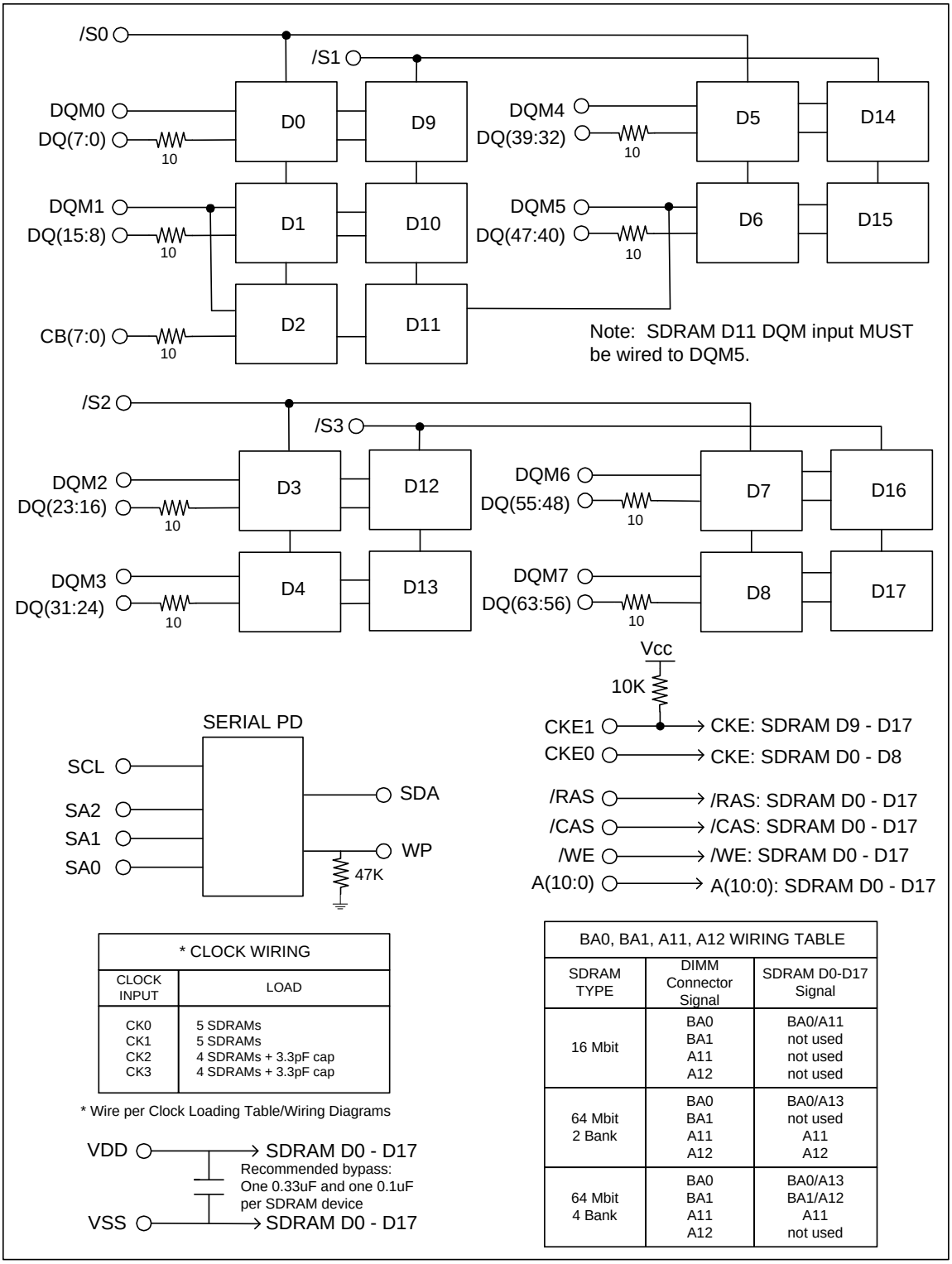


* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	5 SDRAMs TERMINATION 4 SDRAMs + 3.3pF cap TERMINATION

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0-D8 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Figure 12: 72-Bit ECC SDRAM DIMM Block Diagram (1 row x8 SDRAMs)

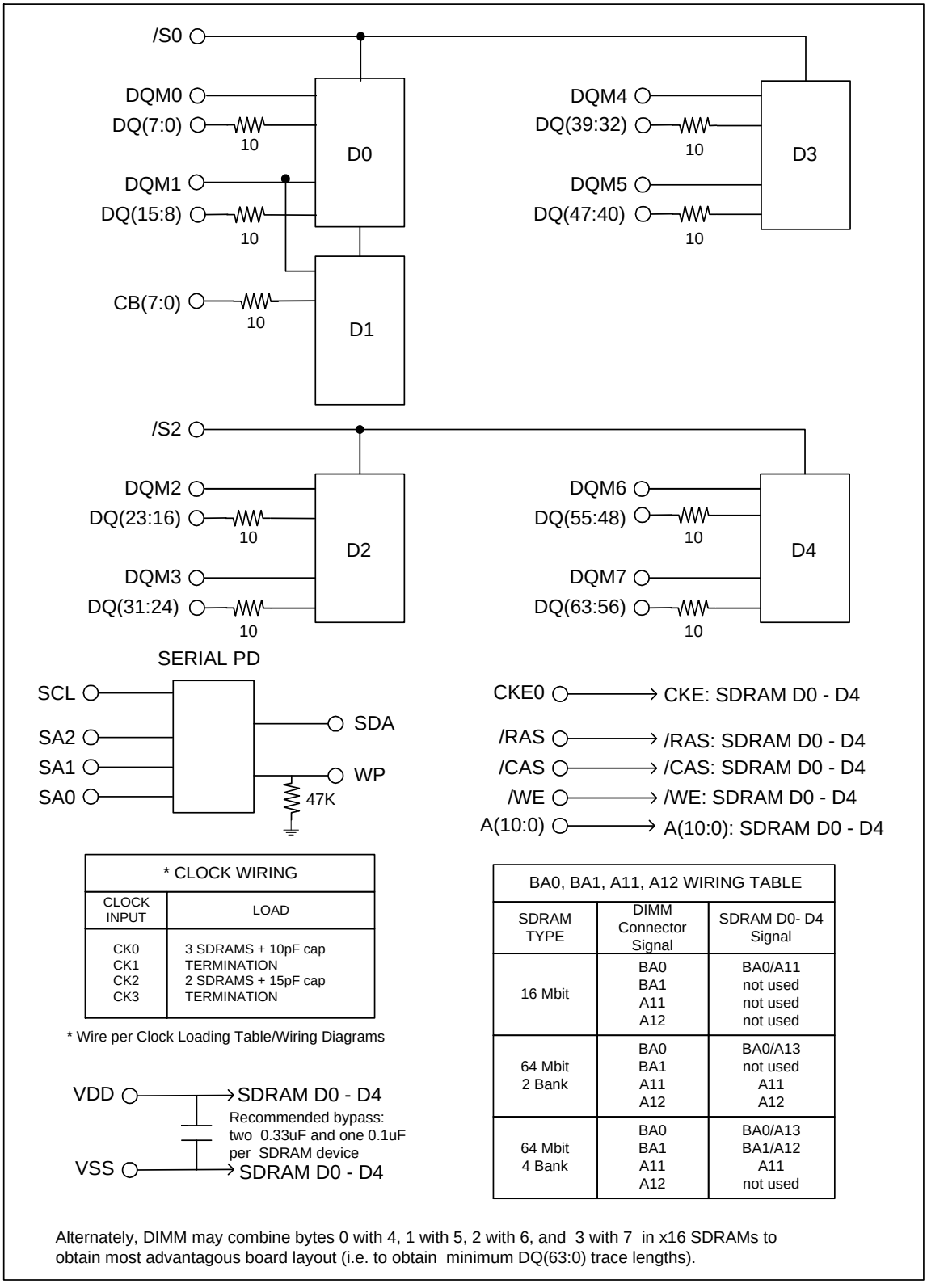


* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0	5 SDRAMs
CK1	5 SDRAMs
CK2	4 SDRAMs + 3.3pF cap
CK3	4 SDRAMs + 3.3pF cap

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0-D17 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Figure 13: 72-Bit ECC SDRAM DIMM Block Diagram (2 rows x8 SDRAMs)



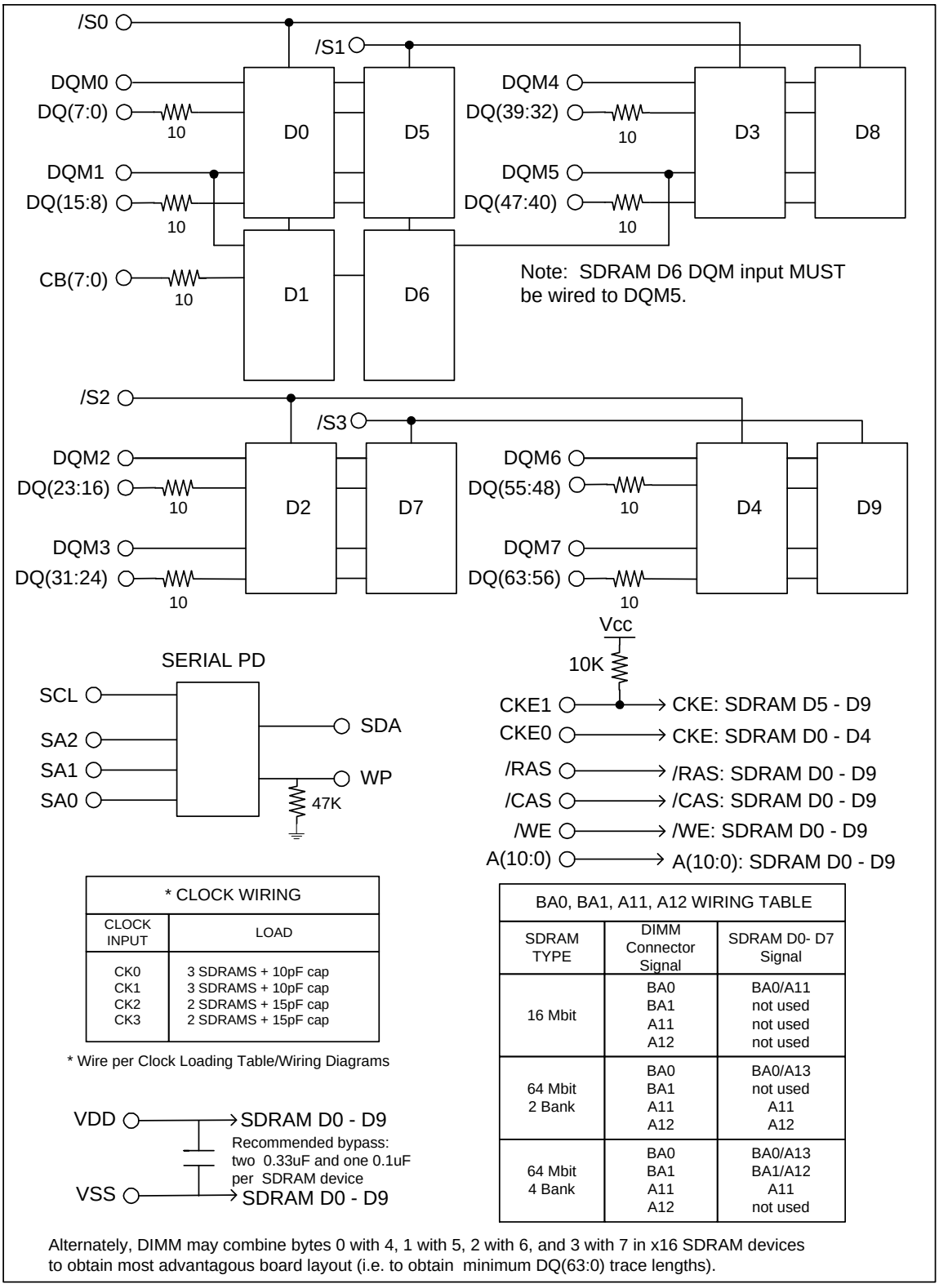
* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	3 SDRAMS + 10pF cap TERMINATION 2 SDRAMS + 15pF cap TERMINATION

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0- D4 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Alternately, DIMM may combine bytes 0 with 4, 1 with 5, 2 with 6, and 3 with 7 in x16 SDRAMs to obtain most advantagous board layout (i.e. to obtain minimum DQ(63:0) trace lengths).

Figure 14: 72-Bit ECC SDRAM DIMM Block Diagram (1 row x16 SDRAMs)



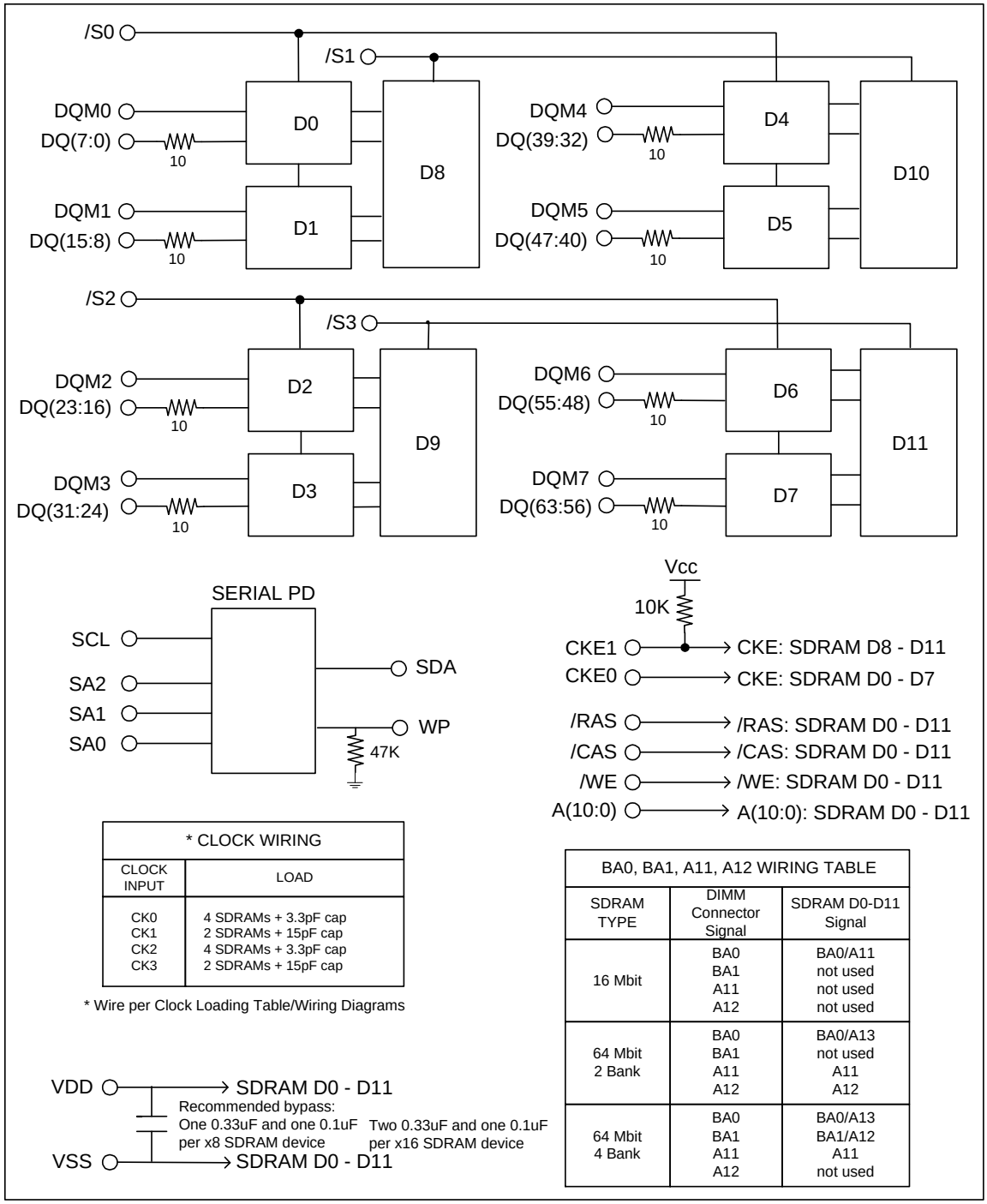
* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0	3 SDRAMS + 10pF cap
CK1	3 SDRAMS + 10pF cap
CK2	2 SDRAMS + 15pF cap
CK3	2 SDRAMS + 15pF cap

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0- D7 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Alternately, DIMM may combine bytes 0 with 4, 1 with 5, 2 with 6, and 3 with 7 in x16 SDRAM devices to obtain most advantagous board layout (i.e. to obtain minimum DQ(63:0) trace lengths).

Figure 15: 72-Bit ECC SDRAM DIMM Block Diagram (2 rows x16 SDRAMs)

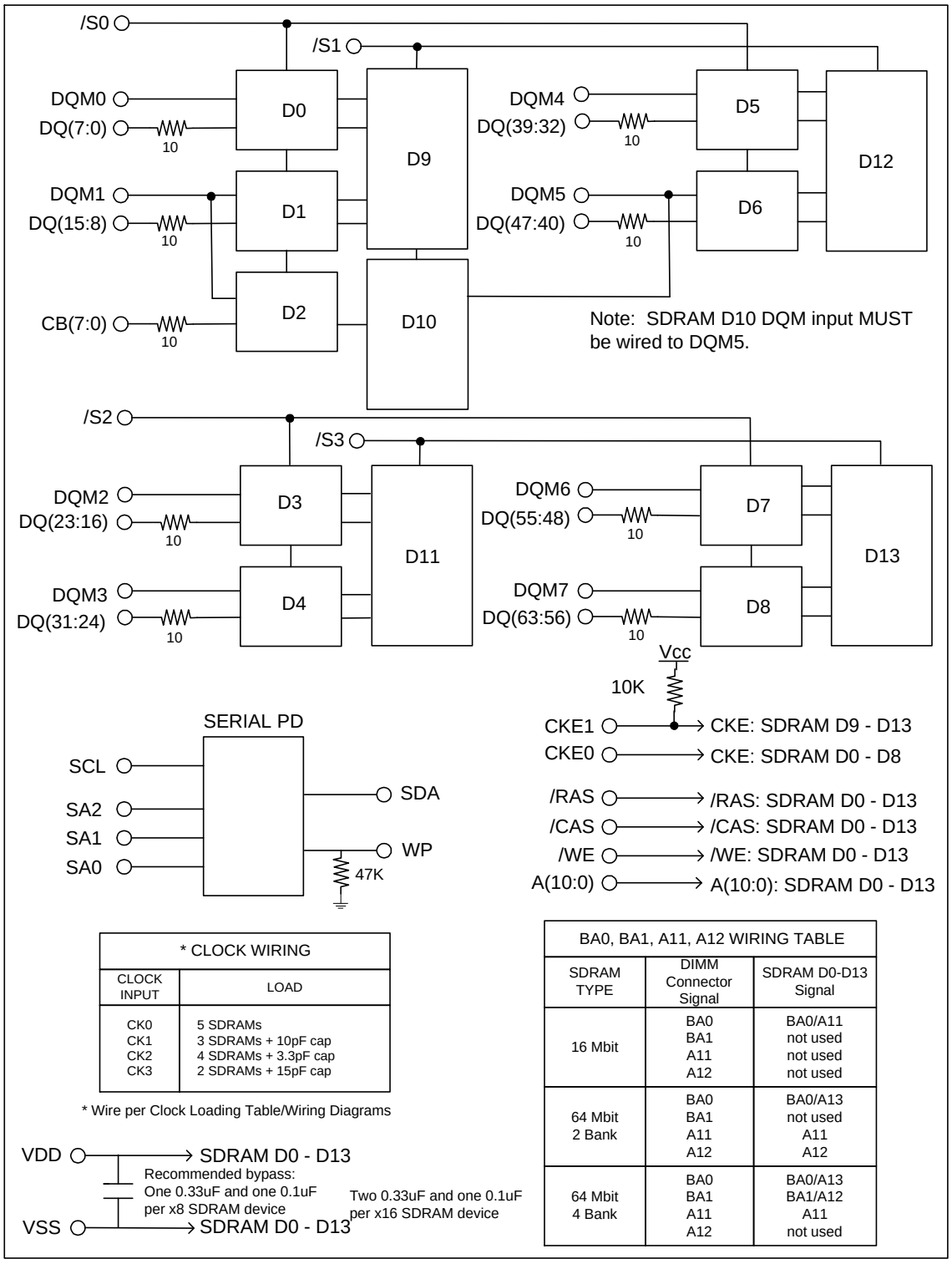


* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	4 SDRAMs + 3.3pF cap 2 SDRAMs + 15pF cap 4 SDRAMs + 3.3pF cap 2 SDRAMs + 15pF cap

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0-D11 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Figure 16: 1 Row x8 + 1 Row x16 SDRAMs DIMM Block Diagram



* CLOCK WIRING	
CLOCK INPUT	LOAD
CK0 CK1 CK2 CK3	5 SDRAMs 3 SDRAMs + 10pF cap 4 SDRAMs + 3.3pF cap 2 SDRAMs + 15pF cap

* Wire per Clock Loading Table/Wiring Diagrams

BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	DIMM Connector Signal	SDRAM D0-D13 Signal
16 Mbit	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A13 not used A11 A12
64 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used

Figure 17: 72-Bit ECC SDRAM DIMM Block Diagram (1 Row x8 + 1 Row x16)

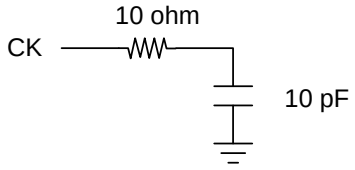
Clock Loading Table:

SDRAM Data Width	# of Rows on DIMM	Total # of SDRAMs	CLK Loading			
			CK0	CK1	CK2	CK3
x8	1	8	4 + 3.3pF cap	*	4 + 3.3pF cap	*
x8	2	16	4 + 3.3pF cap	4 + 3.3pF cap	4 + 3.3pF cap	4 + 3.3pF cap
x16	1	4	2 + 15pF cap	*	2 + 15pF cap	*
x16	2	8	2 + 15pF cap	2 + 15pF cap	2 + 15pF cap	2 + 15pF cap
x32	1	2	2 + TBD cap	*	*	*
x32	2	4	2 + TBD cap	2 + TBD cap	*	*
x8	1	9	5	*	4 + 3.3pF cap	*
x8	2	18	5	5	4 + 3.3pF cap	4 + 3.3pF cap
x16	1	5	3 + 10pF cap	*	2 + 15pF cap	*
x16	2	10	3 + 10pF cap	3 + 10pF cap	2 + 15pF cap	2 + 15pF cap
x8 / x16	2	12	4 + 3.3pF cap	2 + 15pF cap	4 + 3.3pF cap	2 + 15pF cap
x8 / x16	2	14	5	3 + 10pF cap	4 + 3.3pF cap	2 + 15pF cap

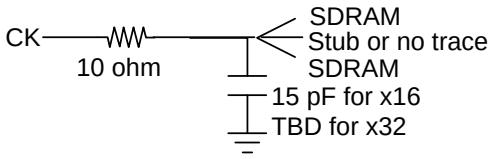
NOTE: ALL CAPS USED IN THE CLOCK NETS MUST HAVE A TOLERANCE OF +/- 5%

* Use termination R/C

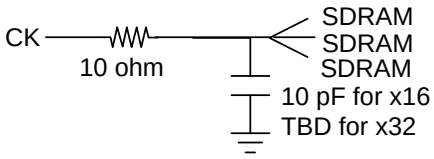
Termination R/C for CK signals not connected to SDRAMs:



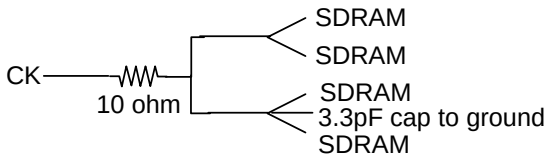
2 Load + TBD cap CK nets:



3 Load + TBD cap CK nets:



4 Load + 3.3pF CK nets:



5 Load CK nets:

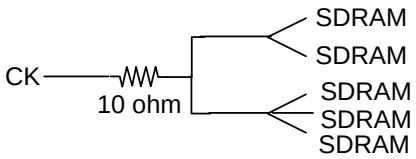


Figure 18: Clock Loading Table & Wiring Diagram

6.0 DIMM PCB Layout and Signal Routing

Printed Circuit Board

The DIMM printed circuit board may be of four or six layer design using glass epoxy material. (However, please note that no information is currently available in this specification for the required lengths of clock traces routed on the outer layers. Such information is yet to be determined.) PCBs must have both a full ground plane layer and full power plane layer. The PCB stackup must be designed to achieve the following calculated board characteristics (assuming 6 mil wide traces) (see example below):

Table 8: PCB Calculated Parameters

Parameter	Min	Max
Propagation delay: S_0 [ns/ft] (outer layers)	1.6	2.2
Propagation delay: S_0 [ns/ft] (inner layers)	2.0	2.2
Trace impedance: Z_0 [Ω] (all layers)	60	80

Required Dielectric: 4.2 to 4.8

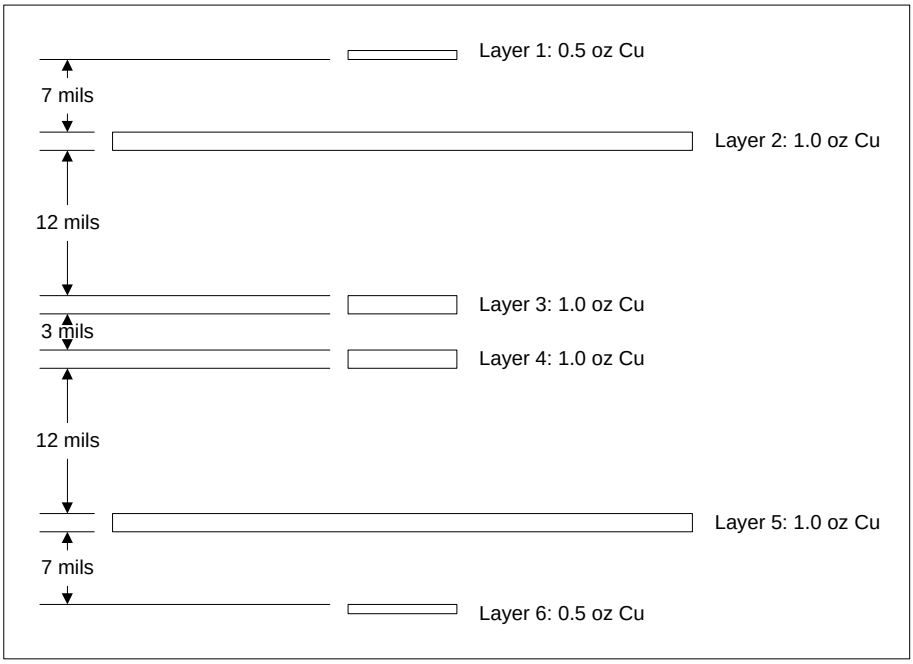


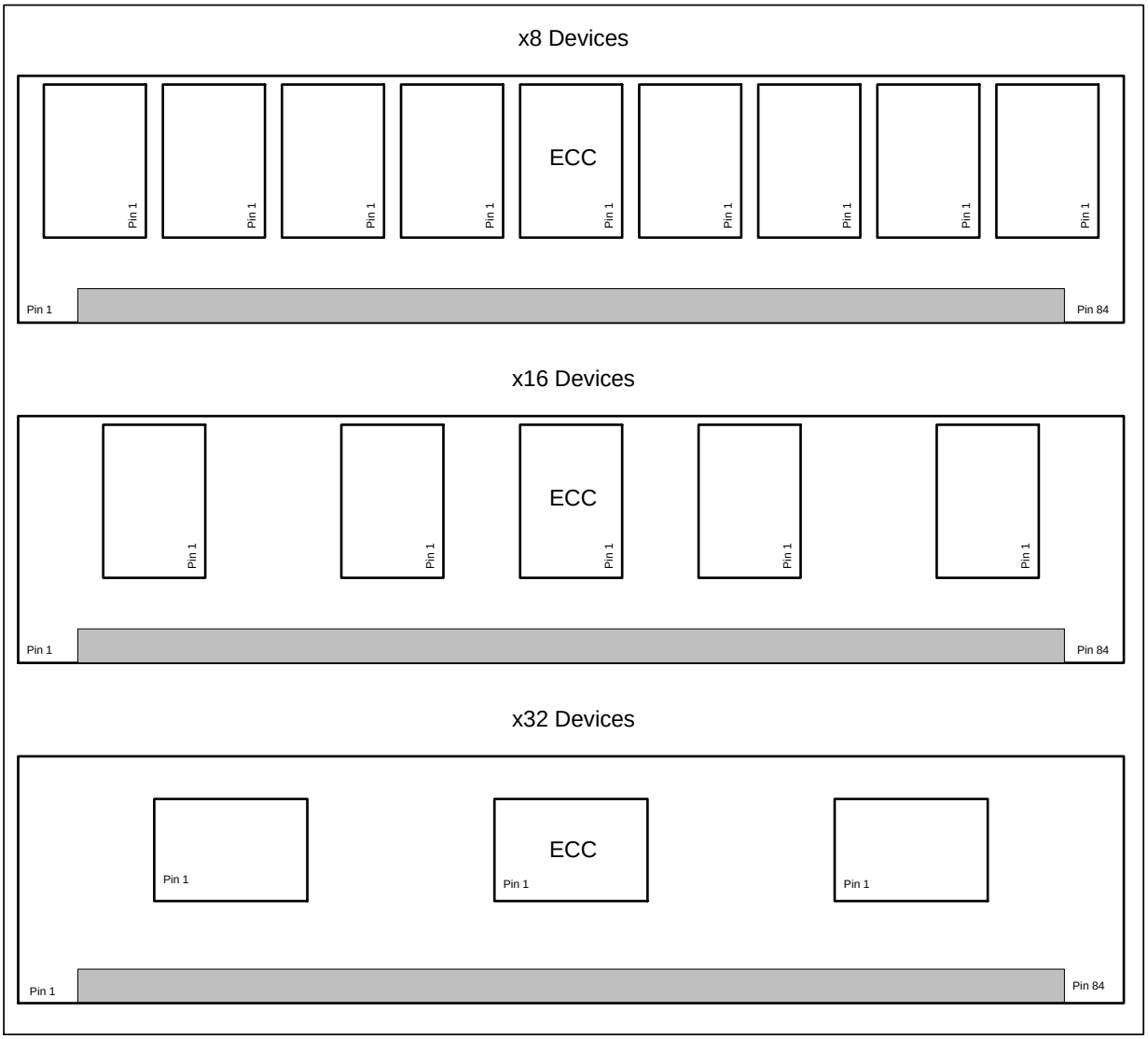
Figure 19: Example 6-layer PCB Stackup

The PCB edge connector contacts shall be gold plated per Figure 5 note 10. Note: The PCB connector edge will not be chamfered. The text “1M X 64 SDRAM”, “2M X 64 SDRAM”, “4M X 64 SDRAM”, “8M X 64 SDRAM” or “16M X 64 SDRAM” (or other appropriate size designation) shall appear in the PCB silk-screen or surface layer etch (or label) as appropriate, together with manufacturer’s name and DIMM assembly part number.

Component Types and Placement

Components shall be of surface mount type, and may be mounted on one or both sides of the PCB. Components shall be positioned on the PCB to meet the min and max trace lengths required for SDRAM data signals. Bypass capacitors for SDRAM devices must be located as near as practical to the device power pins. In two bank SDRAM designs, location of the SDRAM devices and pin swapping of data pins between banks should be used to ensure an absolute minimum of additional data signal trace length due to the second bank.

The following diagram illustrates the suggested placement for x8, x16 and x32 SDRAM devices. For double-sided, non mixed-mode DIMMs, the back side placement should be mirrored from the front side. For mixed-mode DIMMs, the front side x8 placement should be combined with the mirrored back-side x16 placement. The placement for non ECC DIMMs is equivalent to the placements shown below after removing the ECC chips. It is intended that the space for ECC remain intact so that one layout may be used for both ECC and non-ECC cases; however, this is not a requirement. Exact spacing numbers are not provided, but are left up to the DIMM manufacturer to determine based on manufacturing constraints and signal routing constraints imposed by this design guide.



Signal Groups

In this specification, the SDRAM timing-critical signals have been categorized into seven groups. The signals are divided into groups whose members have identical loading and routing topologies. The following table summarizes the signal groups by listing the signals contained in each. The following sections will describe routing restrictions associated with each signal group.

Table 9: Signal Topology Categories

SIGNAL GROUP	SIGNALS IN GROUP
Clock	CK [3:0]
Data	DQ [63:0]
	CB [7:0]
Data Mask (1/2 loads)	DQMB [0,2-4,6,7]
Data Mask (1/2/3 loads)	DQMB [1,5]
Chip Select	CS# [3:0]
Clock Enable	CKE# [0,1]
Double cycle signals	A [12:0]
	BA [0,1]
	RAS#
	CAS#
	WE#

Signal Topology and Length Restrictions

In order to meet signal quality and setup/hold time requirements for the memory interface, certain routing topologies and trace length requirements must be met. The signal topology requirements are shown pictorially in the following pages. Each topology diagram is accompanied by a trace length table that lists either the minimum and maximum lengths allowed for each trace segment or the min and max lengths for the entire net. Each diagram also shows where vias are allowed or includes a note that specifies where vias are allowed that are not shown in the diagram.

Routing Rules

General Info: All signal traces except clocks are routed using 6/10 rules.
(6 mil traces and 10 mil minimum spacing between adjacent traces).

Clocks should be done in 6 mil trace width and 12 mil minimum spacing.

Clocks must be routed with at least 90% of the total trace length in the inner layers.

No test points are required.

Topology Diagram Explanation and Examples

The routing topology diagrams in this section are intended to be used to determine individual signal topologies on a DIMM for any supported configuration. The primary differences in topologies result from using different SDRAM data widths and the choice of whether or not to use ECC.

The way that these diagrams should be read is the following:

Only the cylinders labeled with length designators represent actual physical trace segments. All other lines should be considered zero in length.

All loads and traces outside of the dashed boxes constitute the base topology which covers the minimum loading case for each signal.

Allowed vias are either shown as circles on the topology diagrams or are otherwise documented under each diagram in a separate note.

The topology for a given configuration can be determined by adding the traces and loads within the dashed boxes to the base topology. Add only the traces and loads within boxes that apply for the desired configuration.

Please see the following page for an example of how to use the topology diagrams.

Example: For an 8Mb, single-sided, non-ECC DIMM that uses 16Mbit 1Mx16 SDRAM devices, the resulting topology for MAx,BAx,RAS#,CAS#,WE#, would be the following:

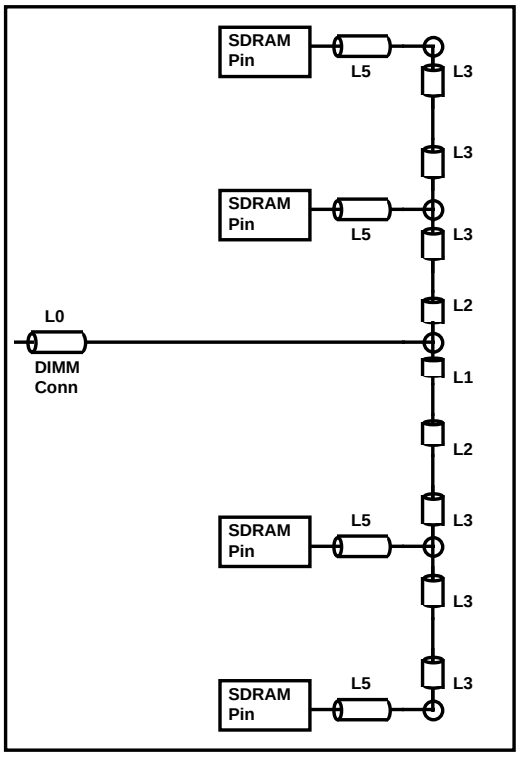


Figure 20: Example Topology

Once the topology has been determined, the permitted segment length ranges for that topology can be read from the table below each topology diagram. It is important to note that some configurations will require more than one topology to account for different numbers of loads on copies of the same signal.

Topology for Clock: CK[3:0]

Special attention must be given to the routing of the SDRAM clock signal(s) to ensure adequate signal quality, rise/fall time, minimum skew between clock edges at each SDRAM component, and predictable skew to motherboard chipset clocks. For that reason, all clocks are made to look electrically like the worst case load (5 loads). Clock signals must have either five SDRAM loads, four SDRAM loads plus an extra 3.3pF cap load or two or three loads plus an extra cap (value depends on x16 or x32 and whether or not ECC is installed on the net). All unused clocks should be terminated into 10 ohms and 10 pF.

DIMMs using all four clocks must have the clocks routed with at least 90% trace length in the inner layers. DIMMs using only two clocks may be routed on the outer layers, but the associated trace lengths will be different. As of this spec revision, the outer layer clock trace lengths are yet to be determined. Clock traces must be 6 mils wide with 12 mil spacing to any other signal including the clocks themselves. The following figure illustrates the recommended clock topologies, and the table on the following page lists required trace segment lengths and added capacitance values and tolerances.

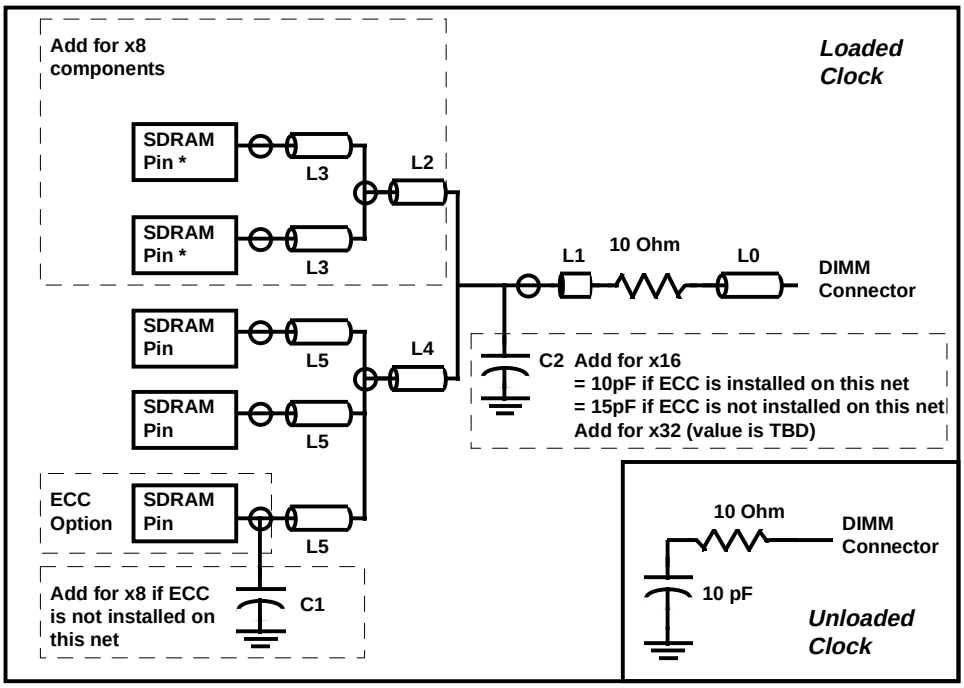


Figure 21: Signal routing topologies for Clocks

Note: The L0 trace segment should contain two vias which are not shown in this diagram. Those vias should be placed near the edge connector and resistor respectively.

Table 10: Trace Length Table for Clock Topologies

Comp Width	Route Layer	SDRAM loads	L0	L1	L2	L3	L4	L5	C1	C2
x32	Outer	2 or 3	TBD	TBD	N/A	N/A	N/A	N/A	TBD	TBD
x16	Outer	2 or 3	TBD	TBD	N/A	N/A	TBD	TBD	TBD	TBD
x8	Outer	4 or 5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	N/A
x32	Inner	2 or 3	TBD	TBD	N/A	N/A	TBD	TBD	TBD	TBD
x16	Inner	2 or 3	0.5	0.11	N/A	N/A	1.2	1.3	0	10pF/15pF
x8	Inner	4 or 5	1.25	0.06	1.20	0.66	0.60	0.66	3.3pF	N/A

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches
2 All capacitances are given in picoFarads and should be kept within a tolerance of +/- 5%

Topology for Data: DQ[63:0] & CB[7:0]

These signals are routed using a balanced "T" topology on any layer. The table defines the line length ranges allowed for these signals. For the purpose of specifying trace segment lengths, the data lines have been broken down into two subcategories based on the location of their edge connector pins. These two data "zones" have lengths specified that make the data lines connecting toward the outside edge shorter in min and max length. This is done to allow the opportunity to pair the necessarily longer data line traces on the motherboard with traces that can be made shorter on the DIMMs, and the necessarily longer DIMM traces with the potentially shorter traces on the motherboard.

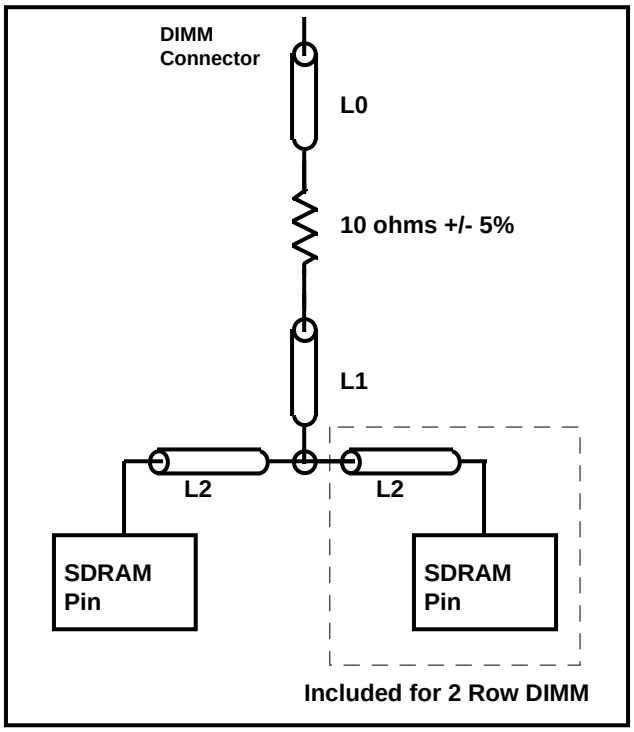


Figure 22: Signal routing topologies for Data

Note: The L0 or L1 trace (but not both) may contain up to 1 additional via which is not shown in the diagram.

Data Zone I : DQ [63-56, 39-24, 7-0]
Data Zone II : DQ [55-40, 23-8] ; CB [7-0]

Table 11: Trace Length Table for Data Topologies

Comp Width	# of loads	Zone	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	Total Min	Total Max
ALL	1/2	I	0.10	0.80	0.10	0.80	0.05	0.15	0.9	1.0
ALL	1/2	II	0.10	1.00	0.10	1.00	0.05	0.15	1.0	1.4

1 All distances are given in inches
2 Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2. Also, the total min and max limits are tighter than the sum of the individual min and max lengths. This implies that not all individual segment lengths may be adjusted to the min or max value respectively at the same time.

Topology for Data Mask (1/2 Loads): DQMB[7,6,4-2,0]

These signals are routed using a " Y" topology on any layer. The tables define the line length ranges allowed for these signals.

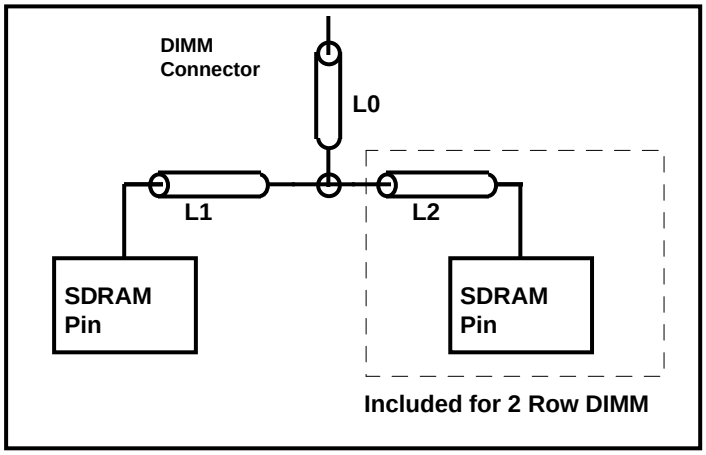


Figure 23: Signal routing topologies for Data Mask (1/2 Loads)

Table 12: Trace Length Table for Data Mask Topologies (1/2 Loads)

Comp Width	# loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max
ALL	1/2	2.00	2.15	0.24	0.30	0.24	0.30

1 All distances are given in inches

Topology for Data Mask (1/2/3 Loads): DQMB[5,1]

These signals are routed using a star topology on any layer. The tables define the line length ranges allowed for these signals.

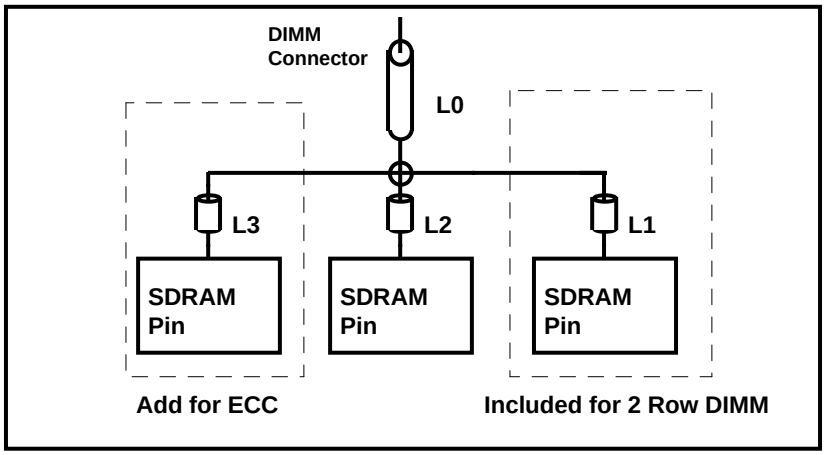


Figure 24: Signal routing topologies for Data Mask (1/2/3 Loads)

Note: The L1, L2 and L3 traces may contain up to 1 additional via each which is not shown in the diagram.

Table 13: Trace Length Table for Data Mask Topologies (1/2/3 Loads)

Comp Width	# loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max
ALL	1/2/3	0.90	1.00	0.63	0.65	0.63	0.65	0.63	0.65

1 All distances are given in inches

Topology for Chip Select: CS#[3:0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for these signals. Diagrams are shown for both cases of a net with an ECC device (or the stuffing option for one) and of a net that does not have an ECC stuffing option.

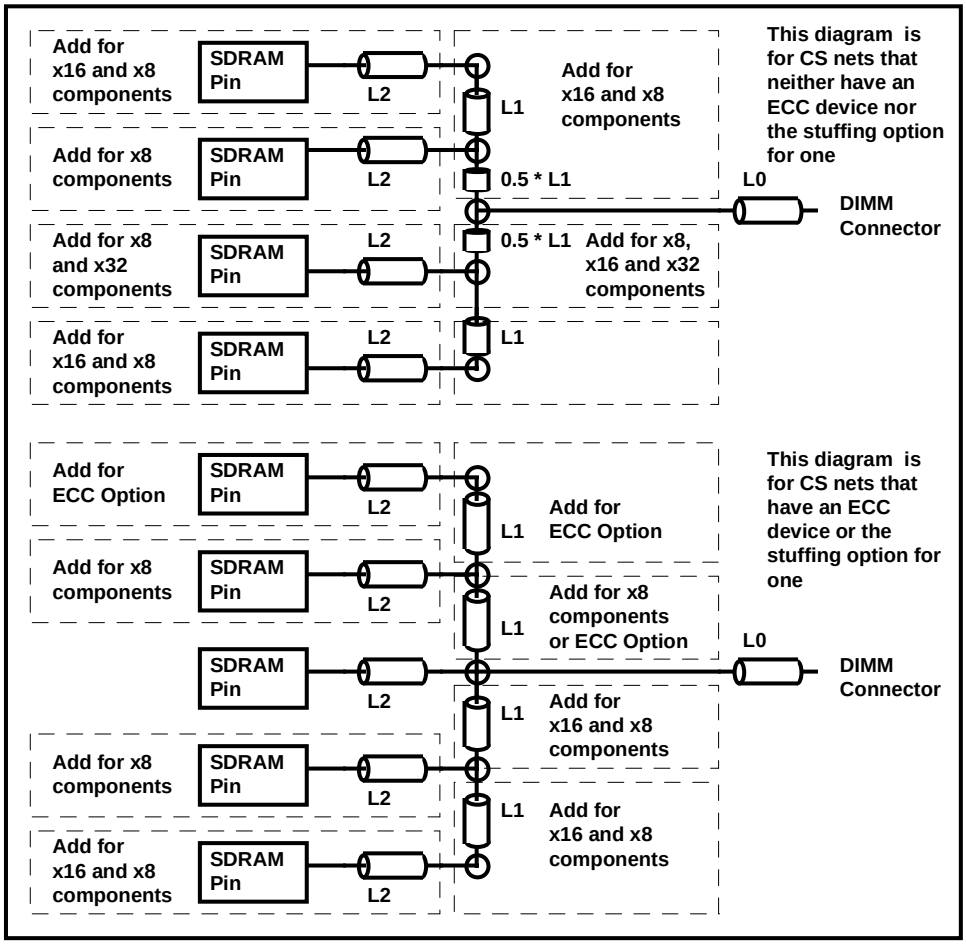


Figure 25: Signal routing topologies for Chip Select

Note: The L0 trace may contain up to 2 vias which are not shown in the diagram. Those vias may be placed anywhere along that trace.

Table 14: Trace Length Table for Chip Select Topologies

Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max
x32	1/2	TBD	TBD	TBD	TBD	TBD	TBD
x16	2/3	1.30	1.65	0.50	0.60	0.06	0.08
x8	4/5	1.30	1.65	0.50	0.60	0.06	0.08

1 All distances are given in inches

Topology for Clock Enable: CKE#[1:0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for each trace segment.

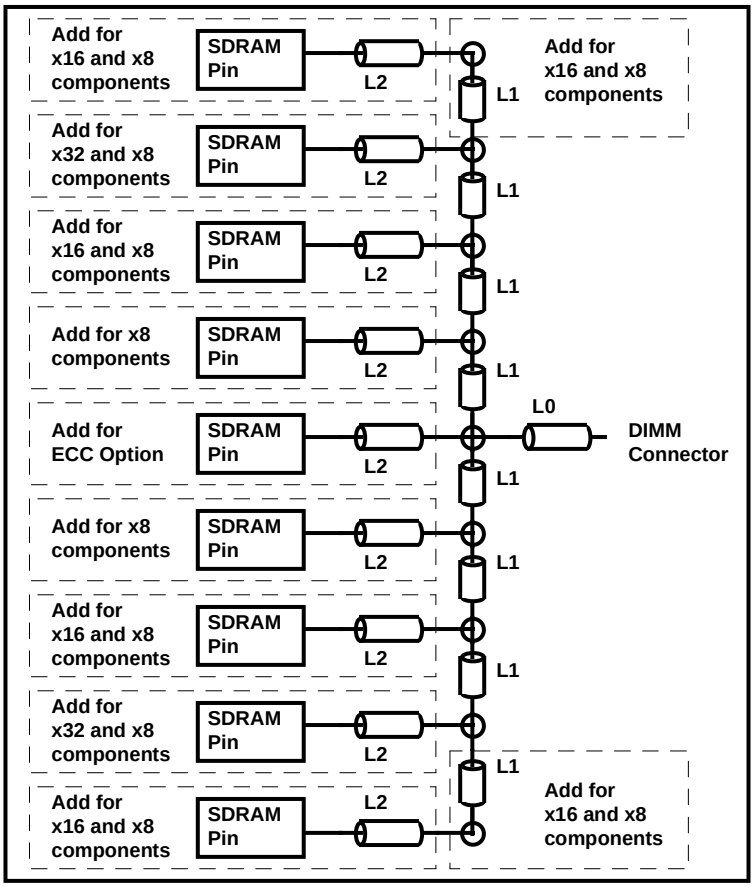


Figure 26: Signal routing topologies for Clock Enable

Note: The L0 trace may contain up to 2 vias which are not shown in the diagram. Those vias may be placed anywhere along that trace.

Table 15: Trace Length Tables for Clock Enable Topologies

Comp Width	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max
ALL	1.40	1.45	0.50	0.60	0.060	0.085

1 All distances are given in inches

Double Cycle Signals: MAx, BAx, SRAS#, SCAS#, WE#

These signals are routed using a balanced, double-sided "comb" topology on any layer. The table below defines the line length ranges allowed for these signals.

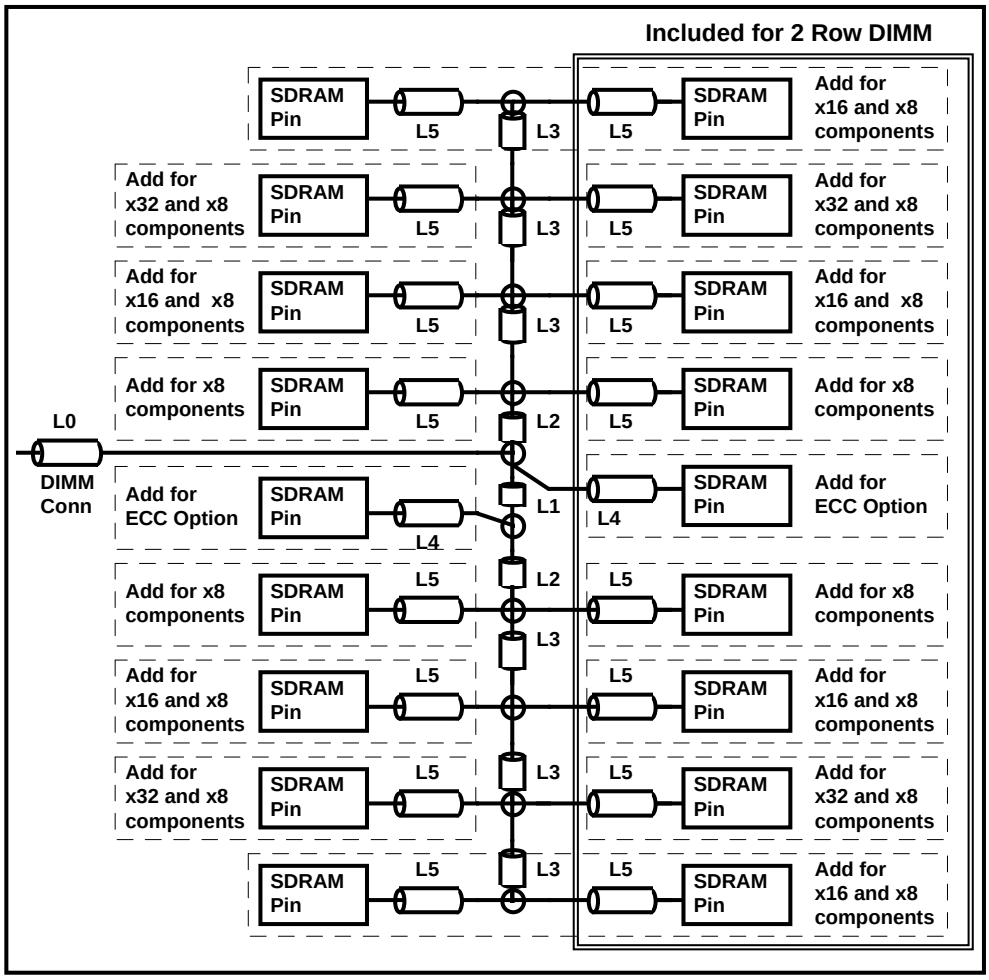


Figure 27: Signal routing topologies for Double Cycle Signals

Note: The L0 trace may contain up to 1 additional via which is not shown in the diagram. That via may be placed anywhere along that trace.

Table 16: Trace Length Table for Double Cycle Signal Topologies

Comp Width	# loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	L4 Min	L4 Max	L5 Min	L5 Max
x32	2/3/4/6	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
x16	4/5/8/10	1.00	1.60	0.20	0.30	0.20	0.55	0.40	0.70	0.05	0.18	0.07	0.35
x8	8/9/16/18	1.00	1.60	0.20	0.30	0.20	0.55	0.40	0.70	0.05	0.18	0.07	0.35

1 All distances are given in inches

7.0 SDRAM Component Specifications

The SDRAM components used with this DIMM design spec MUST adhere to the most recent revision of the Intel “PC/100 SDRAM” Specification. Please reference to that document for all technical specifications and requirements of the SDRAM devices. Any violation of the requirements of the Intel PC/100 SDRAM component spec constitutes a violation of the 100 Mhz Unbuffered SDRAM DIMM specification as well.

8.0 EEPROM Component Specifications

The Serial Presence Detect function is implemented using a 2048 bit EEPROM component such as the National NM24C02L, Catalyst CAT24WC02, SGS Thompson 24C02 or other vendor's equivalent. This nonvolatile storage device contains data programmed by the DIMM manufacturer that identifies the module type and various SDRAM organization and timing parameters. System read/write operations to the EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0) which provide the EEPROM Device Address. The EEPROM device must have an active-high Write Protect input pin, and it must be tied in the non-write protect state on the DIMM PCB through a 47 Kohm pulldown. The EEPROM Write Protect pin should also be connected to pin 81 on the edge connector of the PCB allowing the attached motherboard to control the Write Protect state of the EEPROM. The EEPROM device selected by the DIMM manufacturer must use the SA(2:0) device address signals. The EEPROM must operate with a V_{CC} of 3.0 Vdc to 3.6 Vdc.

In addition to the requirement that the EEPROM meet the functional and electrical specifications listed below, it must also meet the programming requirements specified by the Intel "SDRAM Serial Presence Detect (SPD) Data Structure (168- and SO-144 DIMM)" Specification. Please reference to this document for all programming requirements for the SDRAM SPD EEPROM. Any violation of the requirements of the Intel SDRAM SPD spec constitute a violation of the 100 Mhz DIMM specification as well.

Table 17: EEPROM Component Absolute Maximum Ratings

Parameter	Range
All Input or Output Voltages with Respect to Ground	+4.6V to -0.3V
Ambient Storage Temperature	-50 ^oC to +100 ^oC

Table 18: EEPROM Component Operating Conditions

Parameter	Range
Ambient Operating Temperature	0 ^oC to +70 ^oC
Positive Power Supply	3.0V to 3.6V

Table 19: EEPROM Component A.C. and D.C. Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		5.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		100	uA
I_{LI}	Input Leakage Current	V_{IN} = GND or V_{CC}		10	uA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		10	uA
V_{IL}	Input Low Voltage		-0.3	V_{CC} X 0.3	V
V_{IH}	Input High Voltage		V_{CC} X 0.7		V
V_{OL}	Output Low Voltage	I_{OL} = 3 ma		0.4	V

Table 20: EEPROM Component A.C. Timing Parameters

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	us
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		us
$t_{HD:STA}$	Start Condition Hold Time	4.5		us
t_{LOW}	Clock Low Time	6.7		us
t_{HIGH}	Clock High Time	4.5		us
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		us
$t_{HD:DAT}$	Data In Hold Time	0		us
$t_{SU:DAT}$	Data In Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	us
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		us
t_{DH}	Data Out Hold Time	300		ns
t_{WR}	Write Cycle Time		15	ms

Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the write cycle, the EEPROM bus interface circuits are disabled, SDA remains high due to pull-up resistor, and the EEPROM does not respond to its slave address.

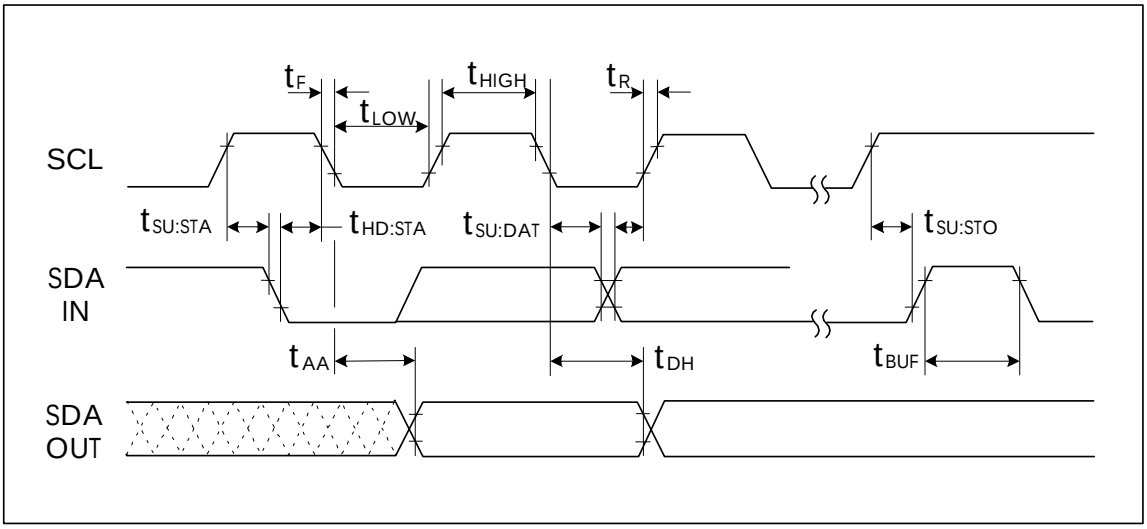


Figure 28: EEPROM Component A.C. Timing Parameters

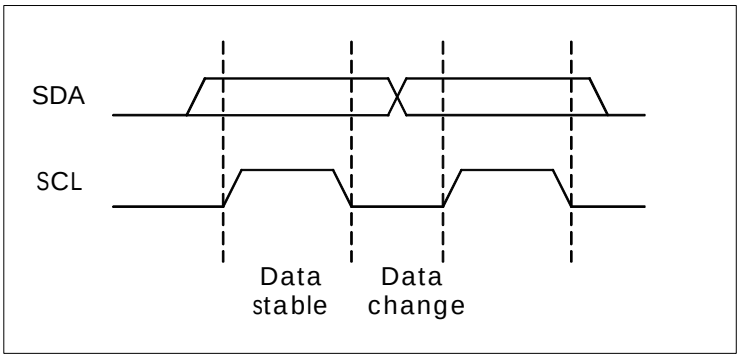


Figure 29: EEPROM Data Validity

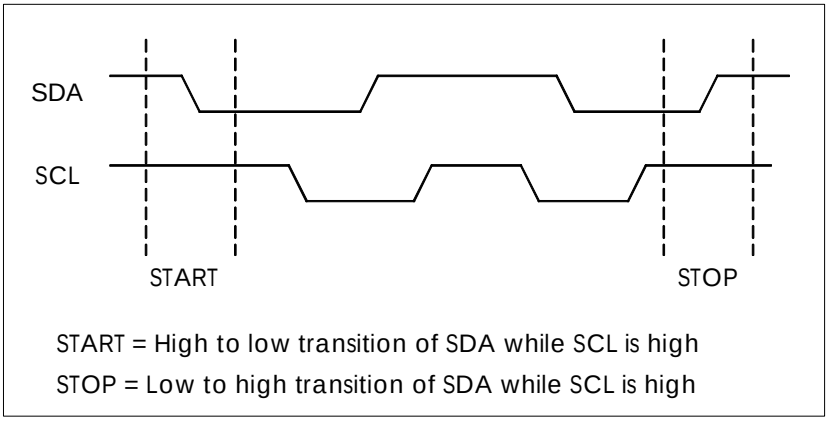


Figure 30: EEPROM Start and Stop conditions

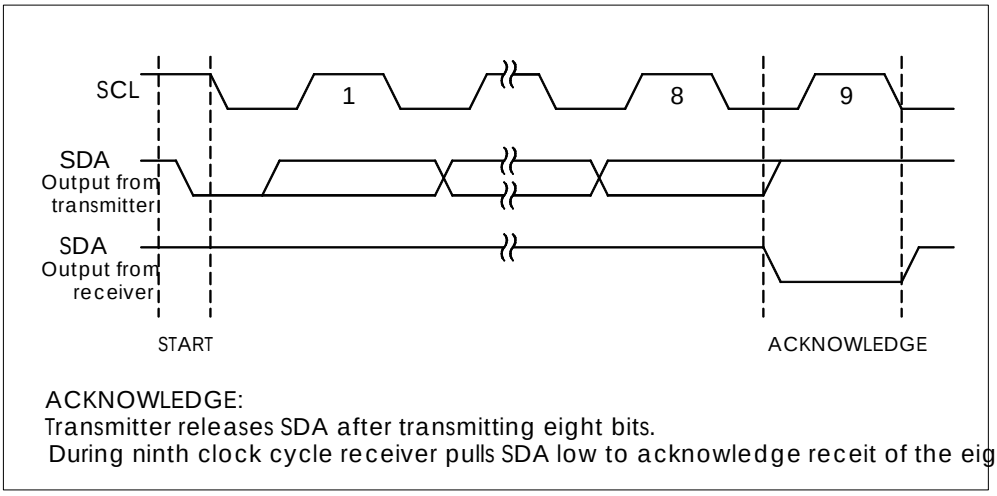


Figure 31: EEPROM Acknowledge

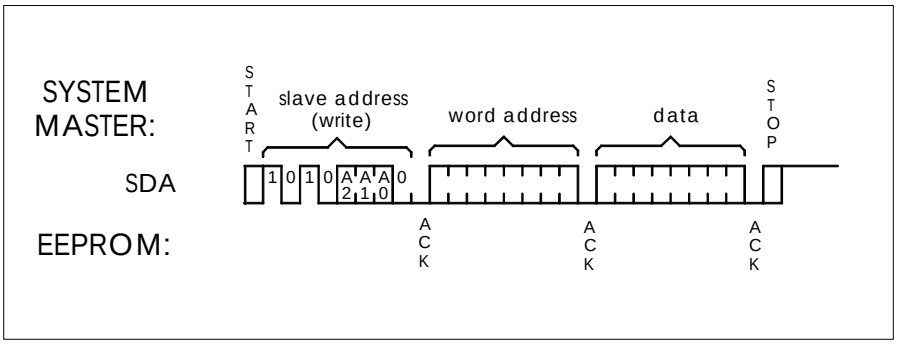


Figure 32: EEPROM Byte Write Operation

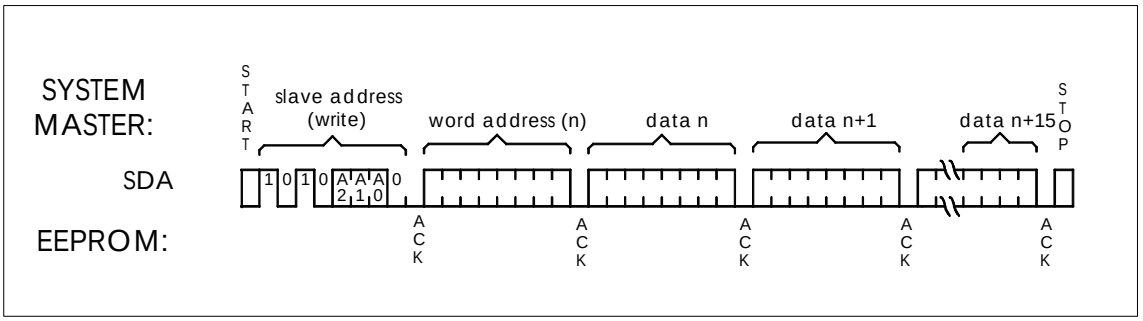


Figure 33: EEPROM Page Write Operation

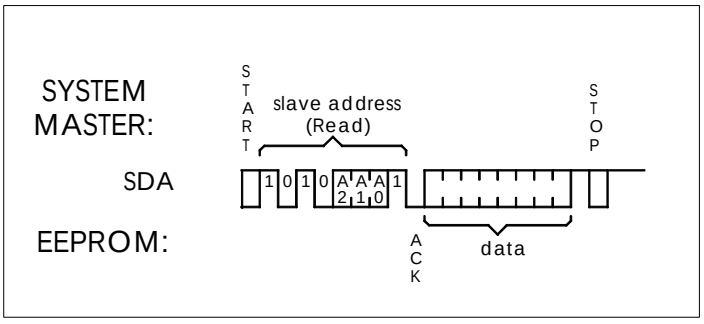


Figure 34: EEPROM Current Address Read Operation

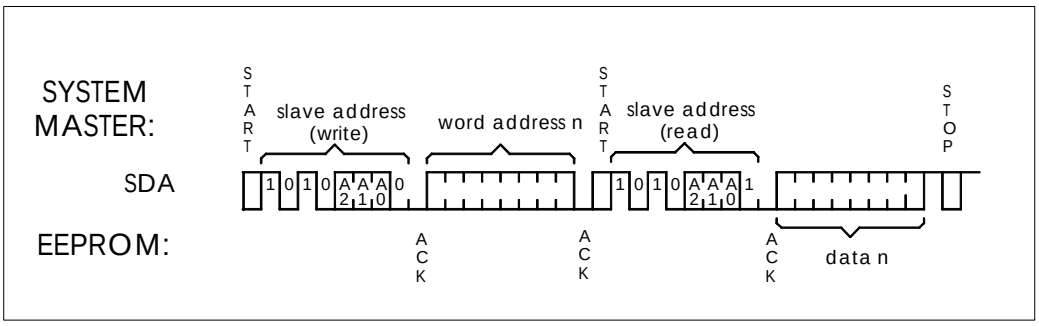


Figure 35: EEPROM Random Read Operation

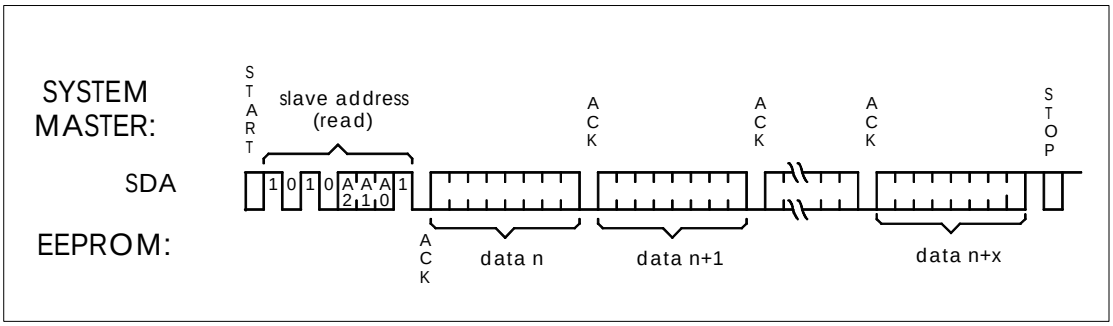


Figure 36: EEPROM Sequential Read Operation